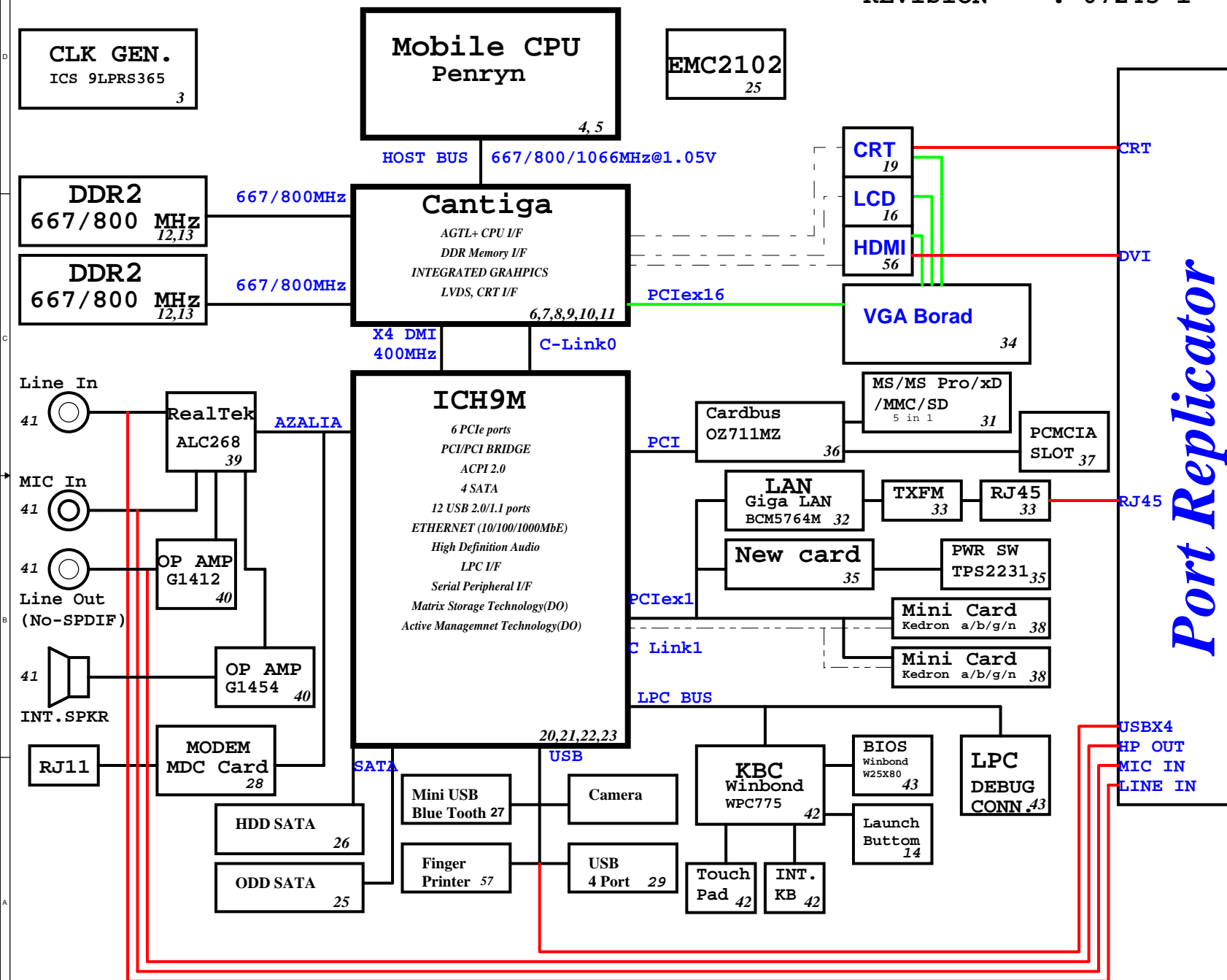


Homa (TM15") Block Diagram

Project code: 91.4Z401.001
PCB P/N : 48.4Z401.011
REVISION : 07245-1



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC TPS51125 49	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(7A) 3D3V_S5(7A)
SYSTEM DC/DC TPS51124 51	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(16A) 1D8V_S3(16A)
TPS51100 50	
5V_S5	DDR_VREF_S3 (1.5A) DDR_VREF_S3_1
G9131	
3D3V_S0	2D5V_S0 (300mA)
APL5912 50	
1D8V_S3	1D5V_S0 (2.5A)
CHARGER BQ24750 53	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA
CPU DC/DC ISL6266A 48	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 38A
GFX DC/DC ISL6263 48	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 5.5A

970

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Title	
BLOCK DIAGRAM	
Size A3	Document Number
Homa	
Date: Thursday, April 03, 2008	Sheet 1 of 57
Rev	-1

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config 1bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIe config 1 bit 0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIe config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved, Rising Edge of PWROK.	This signal has a weak internal pull-down. This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	Tying this strap low configures DMI for ESI-compatible operation. This signal has a weak internal pull up. ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h: bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing. It has a weak internal pull up.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5 page 97

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 10K
DPRSPLVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native CFG9 LAN DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LAD[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1066 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note2) 1 = The iTPM Host Interface is disabled (default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIe Graphics Lane	0 = Reverse Lanes, 15->0, 14->1 ect.. 1 = Normal operation (Default): Lane Numbered in order
CFG10	PCIe Loopback enable	0 = Enable (Note 3) 1 = Disabled (default)
CFG12	ALLZ	0 = ALLZ mode enabled (Note 3) 1 = Disabled (default)
CFG13	XOR	0 = XOR mode enabled (Note 3) 1 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH -> ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH -> ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIe is operational (Default) 1 = Digital display Port and PCIe are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIe disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

3. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

SMBus

USB Table

USB	
Pair	Device
0	USB1
1	USB4
2	USB2
3	DOCK USB
4	USB3
5	Bluetooth
6	FP
7	MINIC1
8	WEBCAM
9	NEW1
10	MINIC2
11	NC

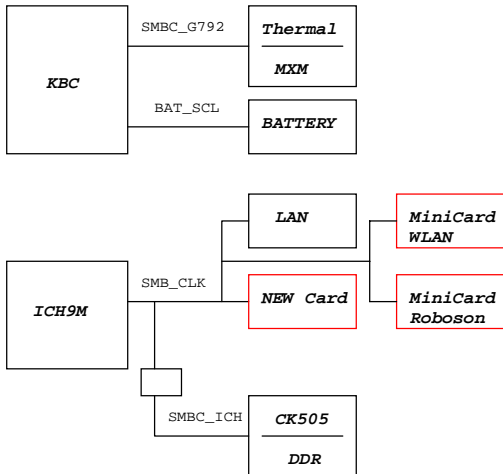
PCI Routing

page 31

	IDSEL	INT	REQ	GNT
RTS5158	AD25	G: CARDBUS	0	0

PCIe Routing

LANE1	LAN BCM5764MKMLG
LANE2	MiniCard WLAN
LANE3	MiniCard Roboson
LANE4	NewCard

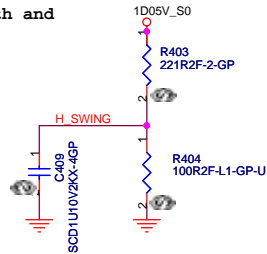


WWW.AliSaler.Com

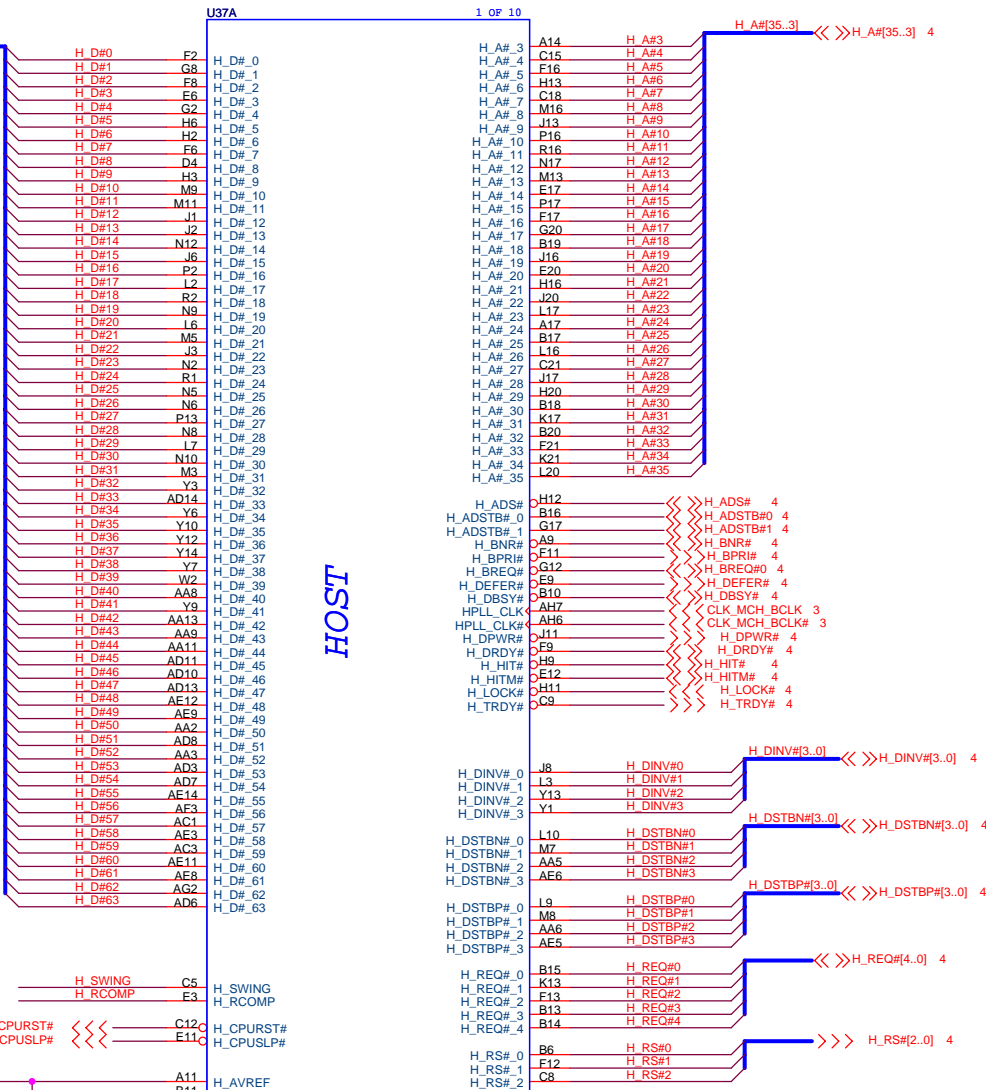
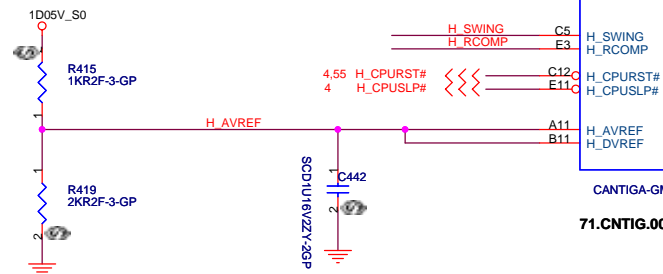
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Title	
Reference	
Size A3	Document Number
Homa	
Date: Thursday, April 03, 2008	Sheet 2 of 57
Rev -1	

H_SWING Resistors and
Capacitors close MCH
500 mil (MAX)

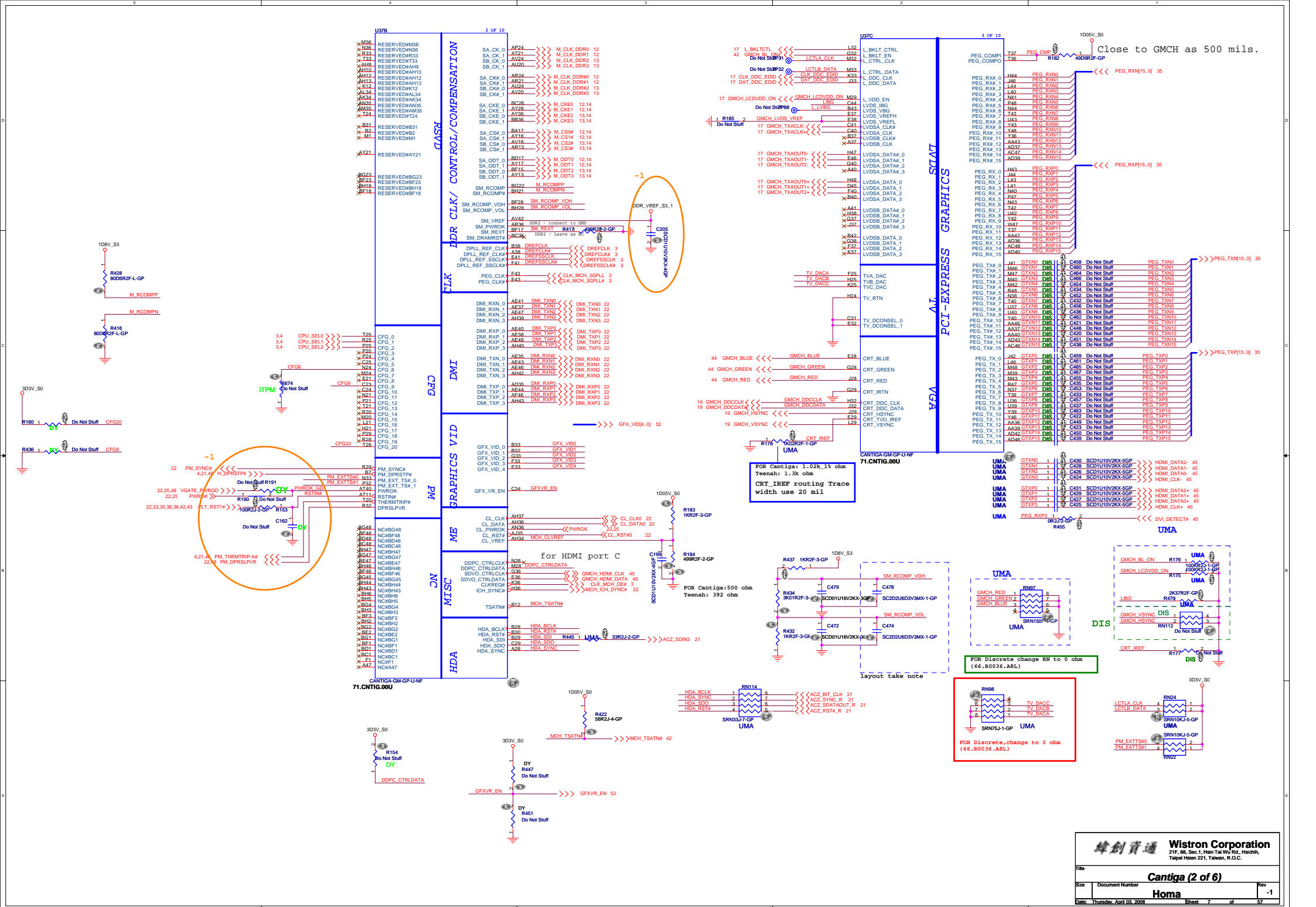


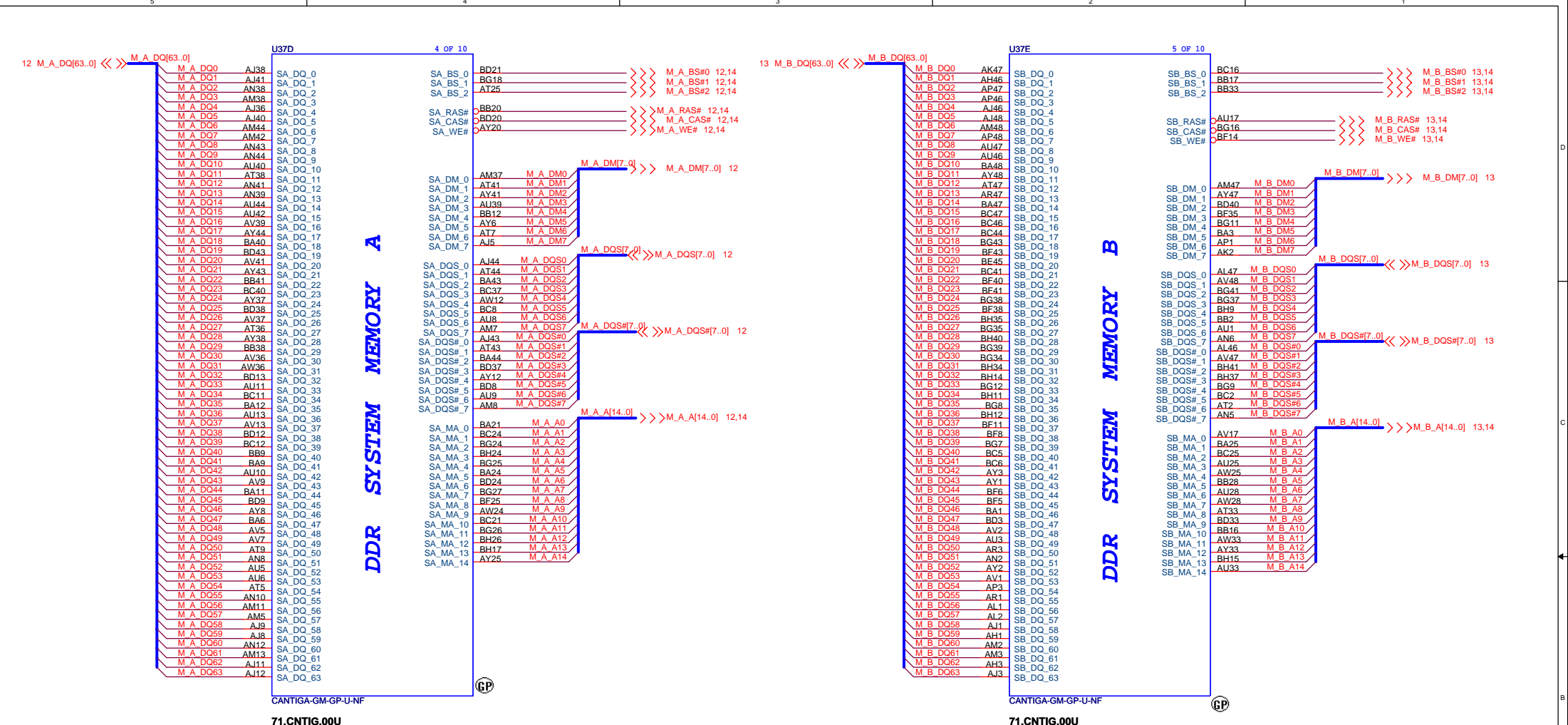
Place them near to the chip (< 0.5")



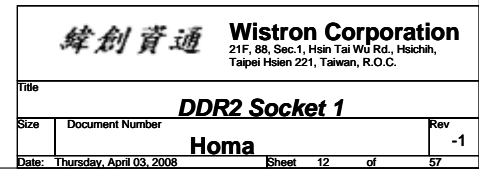
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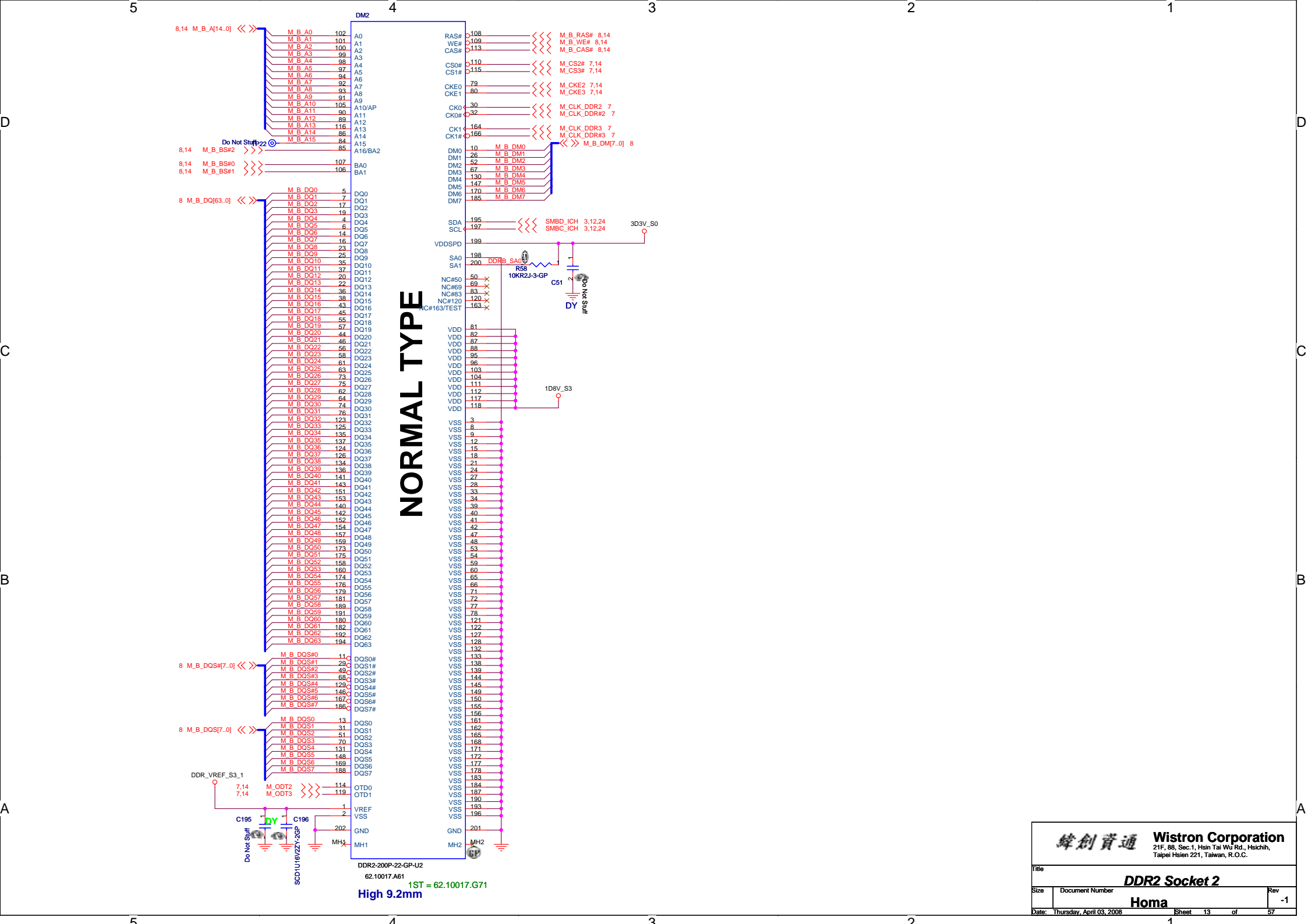
71.CNTIG.00U





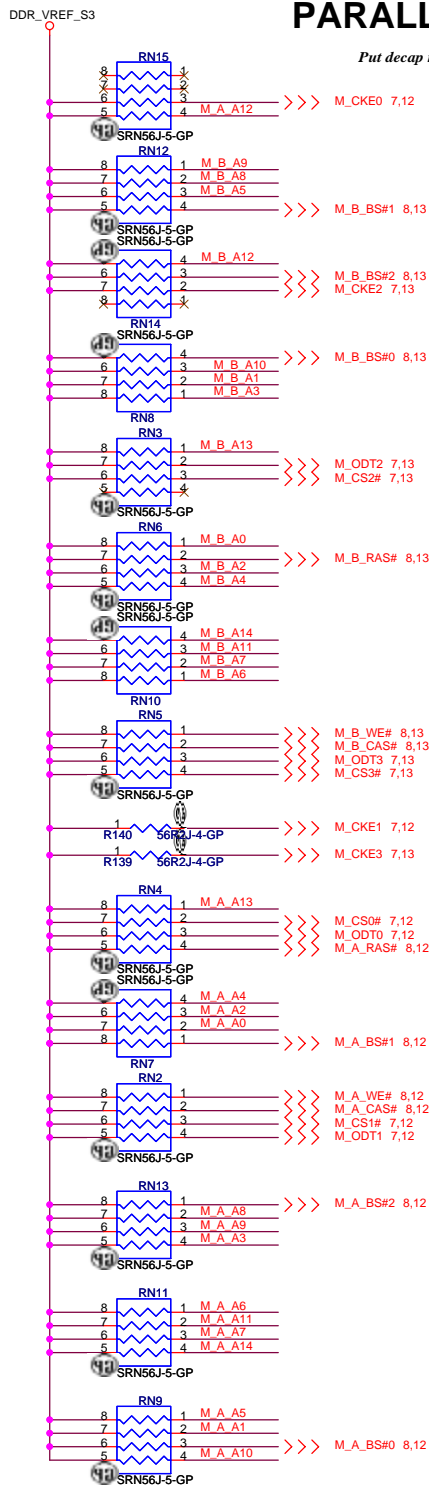






PARALLEL TERMINATION

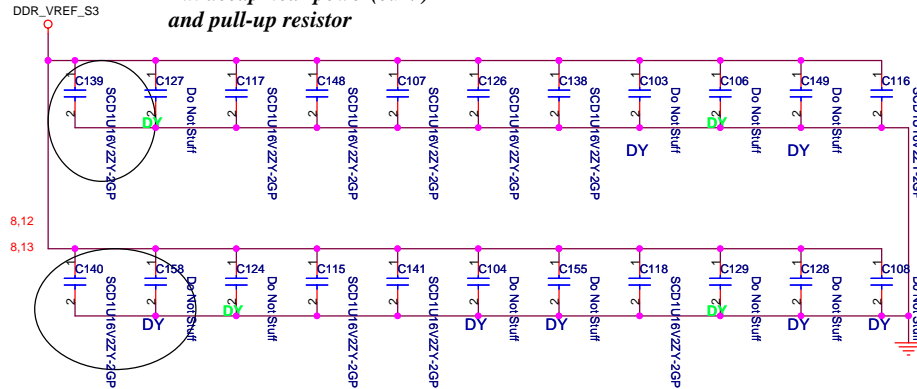
Put decap near power(0.9V) and pull-up resistor



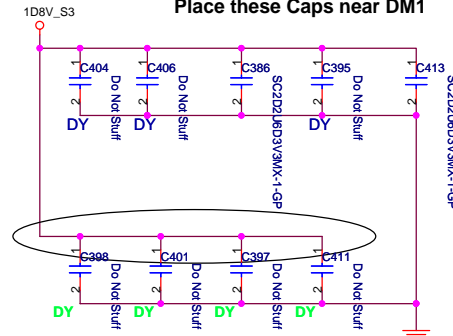
M_A_A[14..0] << M_A_A[14..0] 8,12
M_B_A[14..0] << M_B_A[14..0] 8,13

Decoupling Capacitor

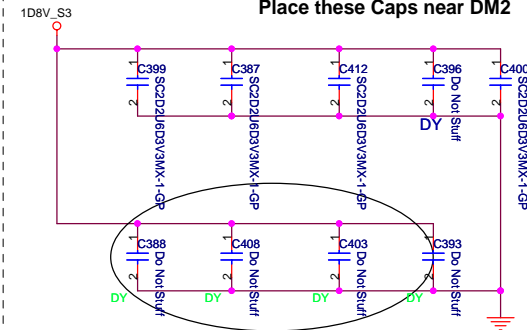
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1

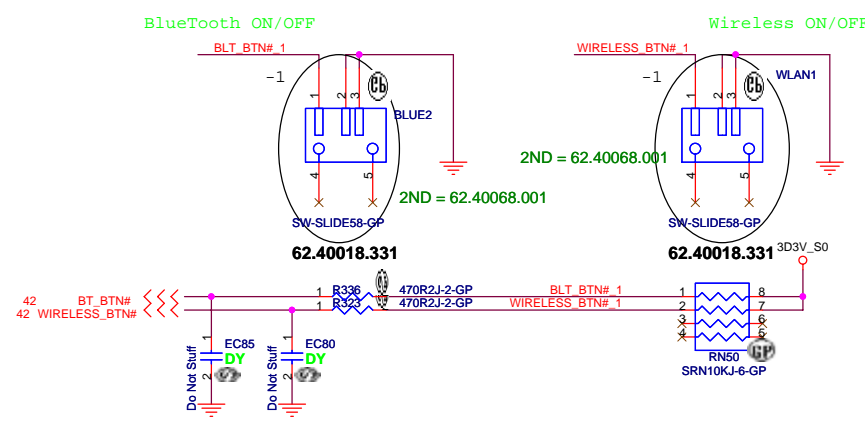


Place these Caps near DM2



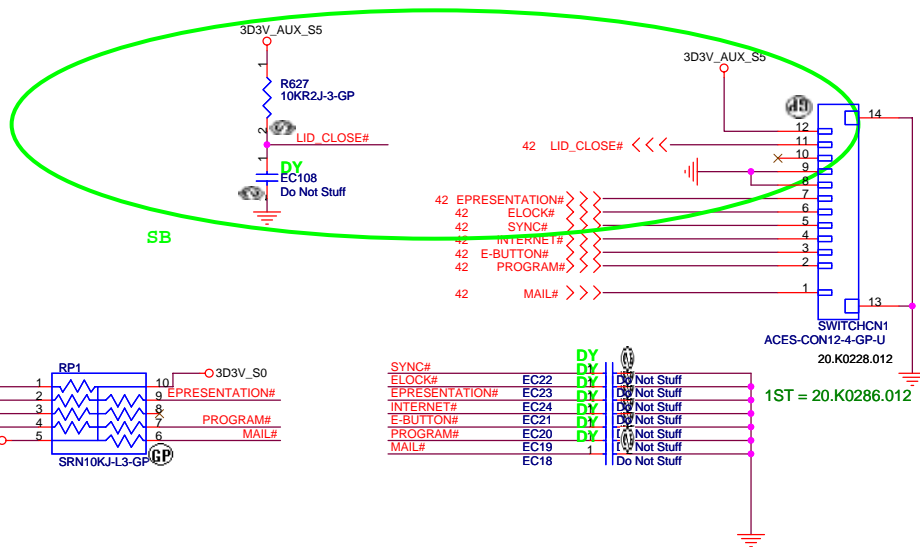
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Size	Document Number	Homa	Rev -1
Date:	Thursday, April 03, 2008	Sheet 14 of 57	

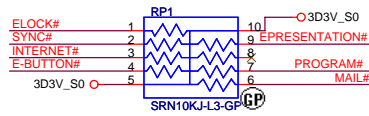


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Title			
SWITCH			
Size	Document Number		Rev
	Homa		-1
Date:	Thursday, April 03, 2008		Sheet 15 of 57



3D3V_AUX_S5	1	TP119	Do Not Stuff
LID_CLOSE#	1	TP121	Do Not Stuff
SYNC#	1	TP120	Do Not Stuff
ELOCK#	1	TP122	Do Not Stuff
EPRESENTATION#	1	TP124	Do Not Stuff
INTERNET#	1	TP123	Do Not Stuff
E-BUTTON#	1	TP126	Do Not Stuff
PROGRAM#	1	TP125	Do Not Stuff
MAIL#	1	TP127	Do Not Stuff



SYNC#	DY	Do Not Stuff
ELOCK#	EC22	Do Not Stuff
EPRESENTATION#	EC23	Do Not Stuff
INTERNET#	EC24	Do Not Stuff
E-BUTTON#	EC21	Do Not Stuff
PROGRAM#	EC20	Do Not Stuff
MAIL#	EC19	Do Not Stuff
	EC18	Do Not Stuff

SWITCHCN1
ACES-CON12-4-GP-U
20.K0228.012

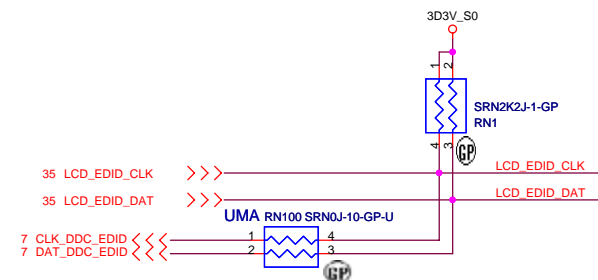
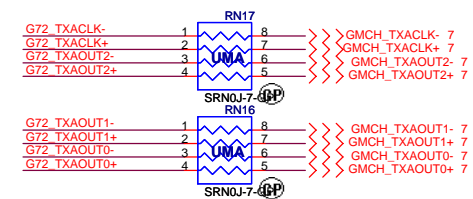
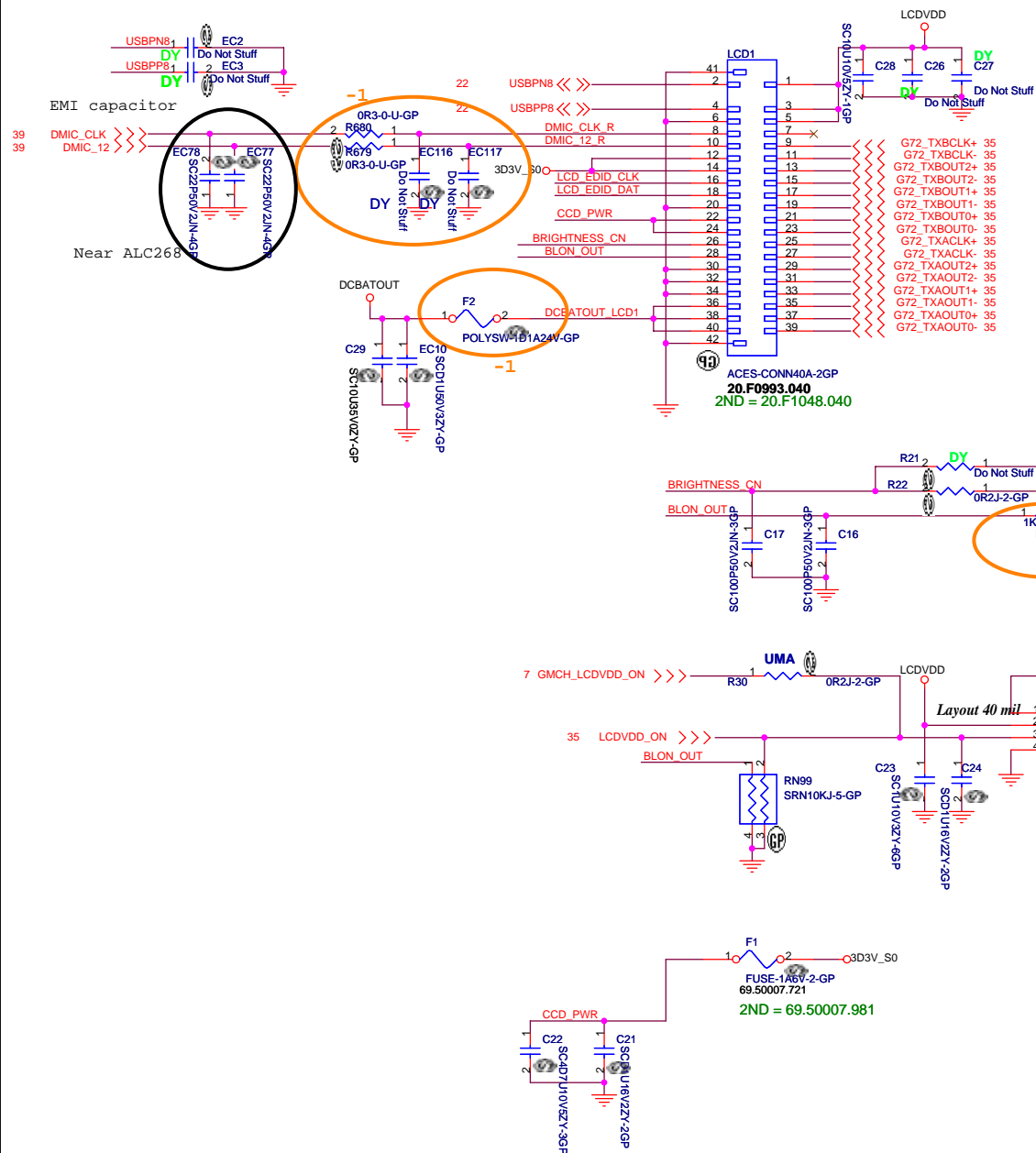
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970

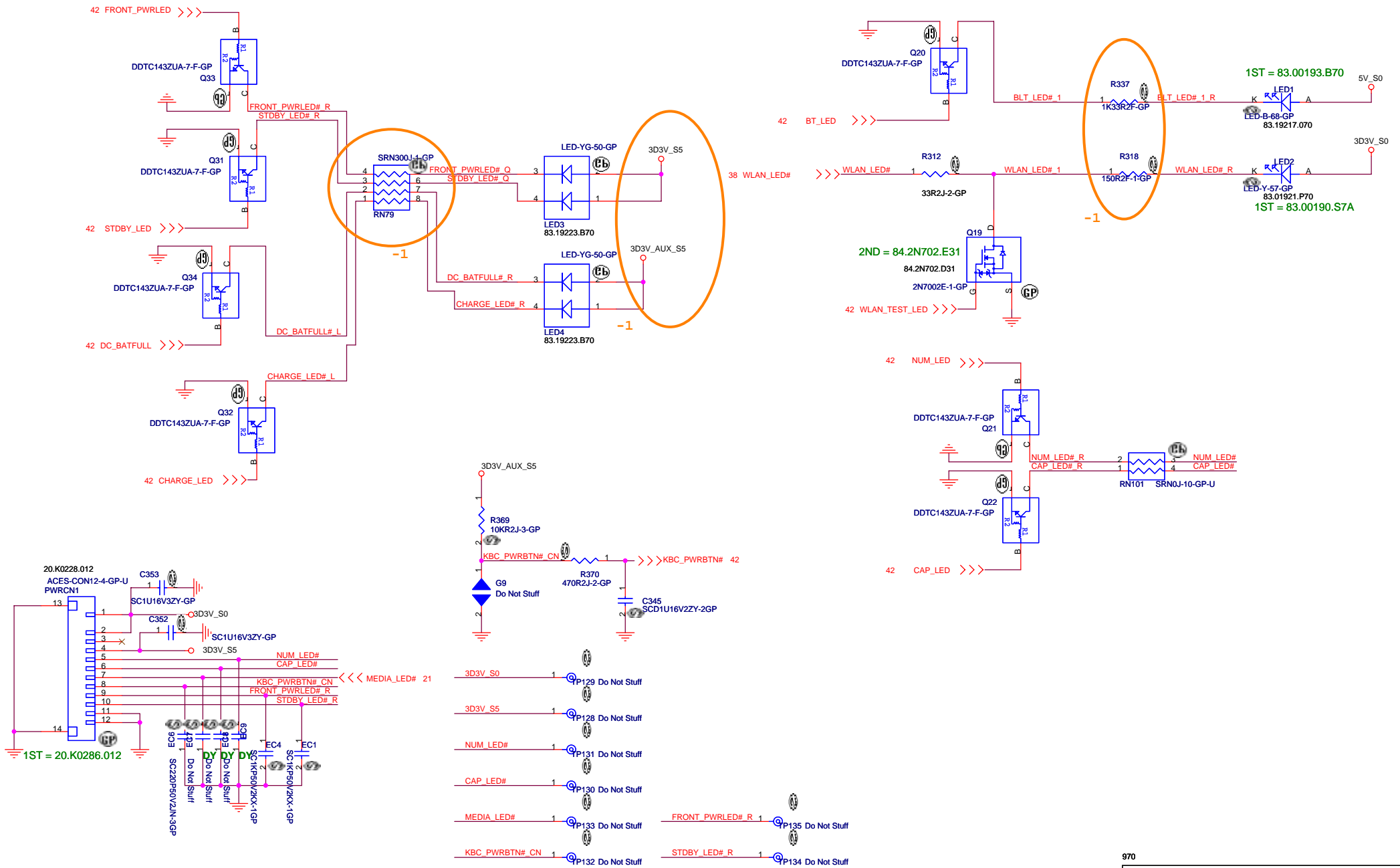
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Title		LAUNCH	
Size	Document Number	Homa	Rev -1
Date:	Thursday, April 03, 2008	Sheet 16 of 57	

LCD/INVERTER/CCD CONN



LED

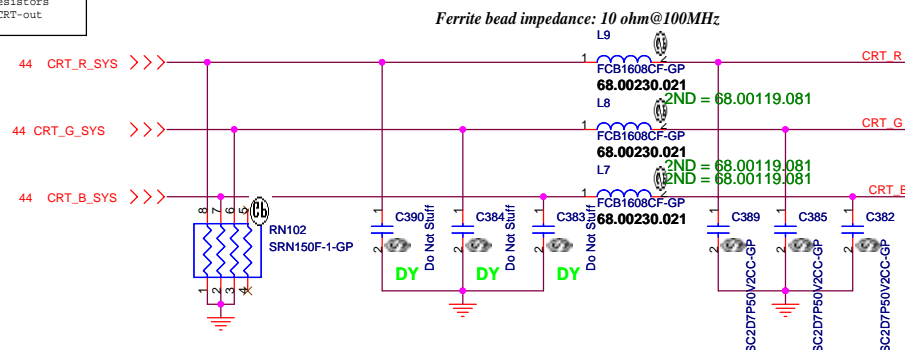


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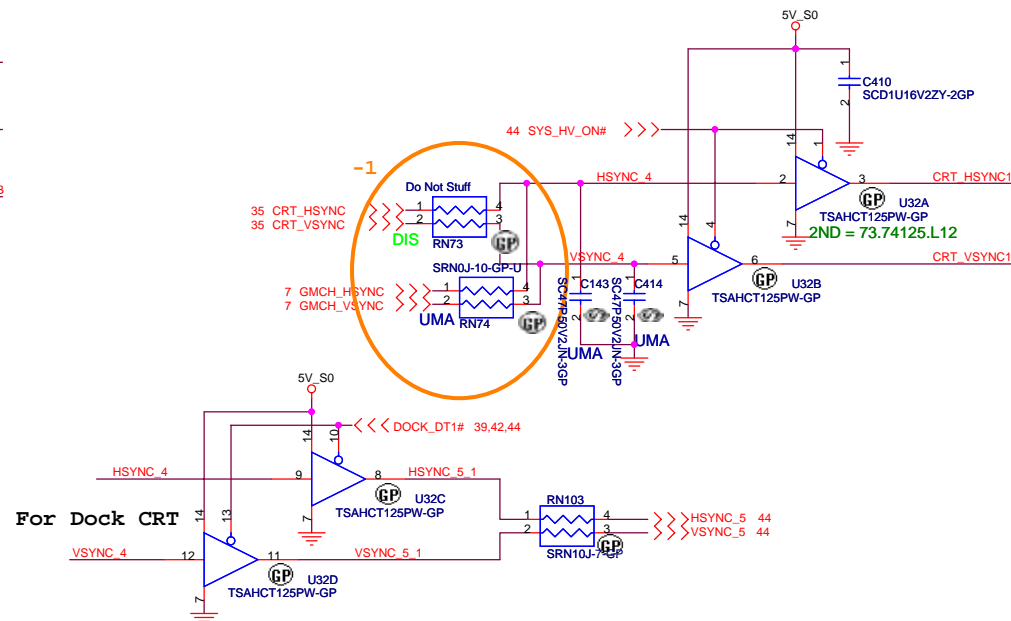
Title			
LED			
Size	Document Number		Rev
	Homa		-1
Date:	Thursday, April 03, 2008		Sheet 18 of 57

Layout Note:
Place these resistors
close to the CRT-out
connector

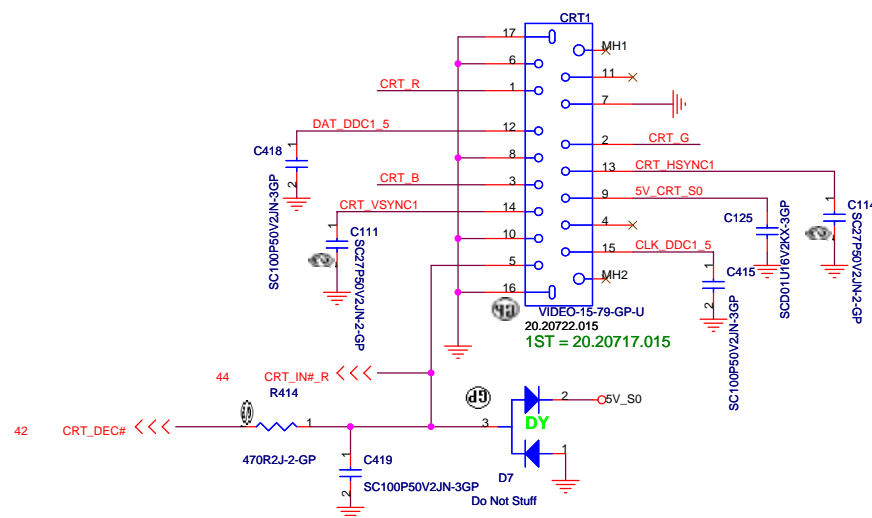


Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

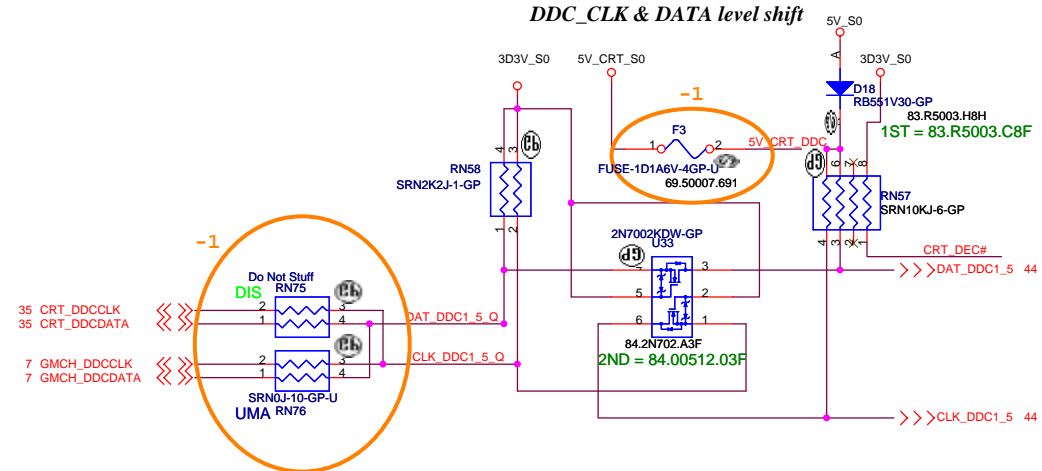
Hsync & Vsync level shift



CRT I/F & CONNECTOR



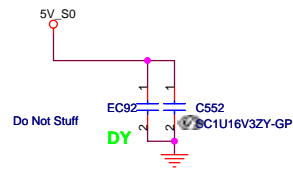
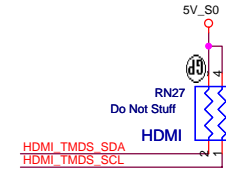
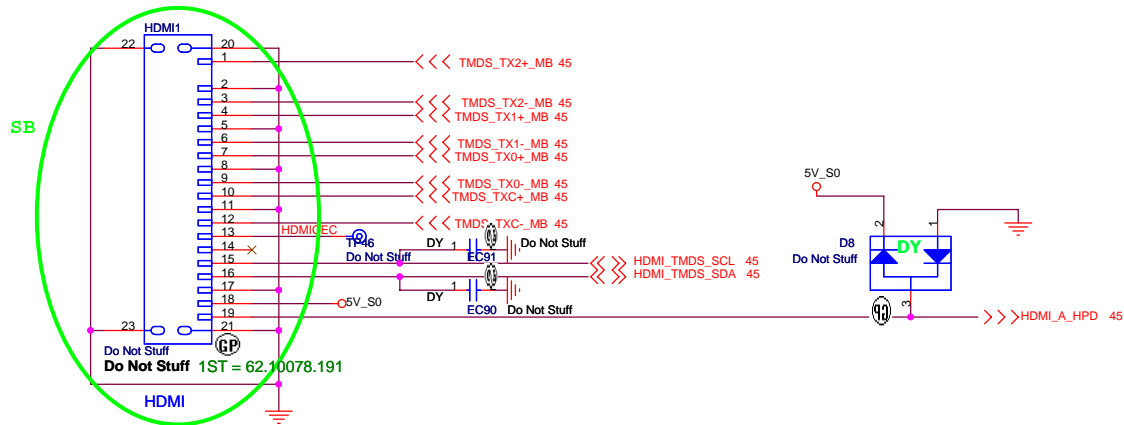
DDC_CLK & DATA level shift



970

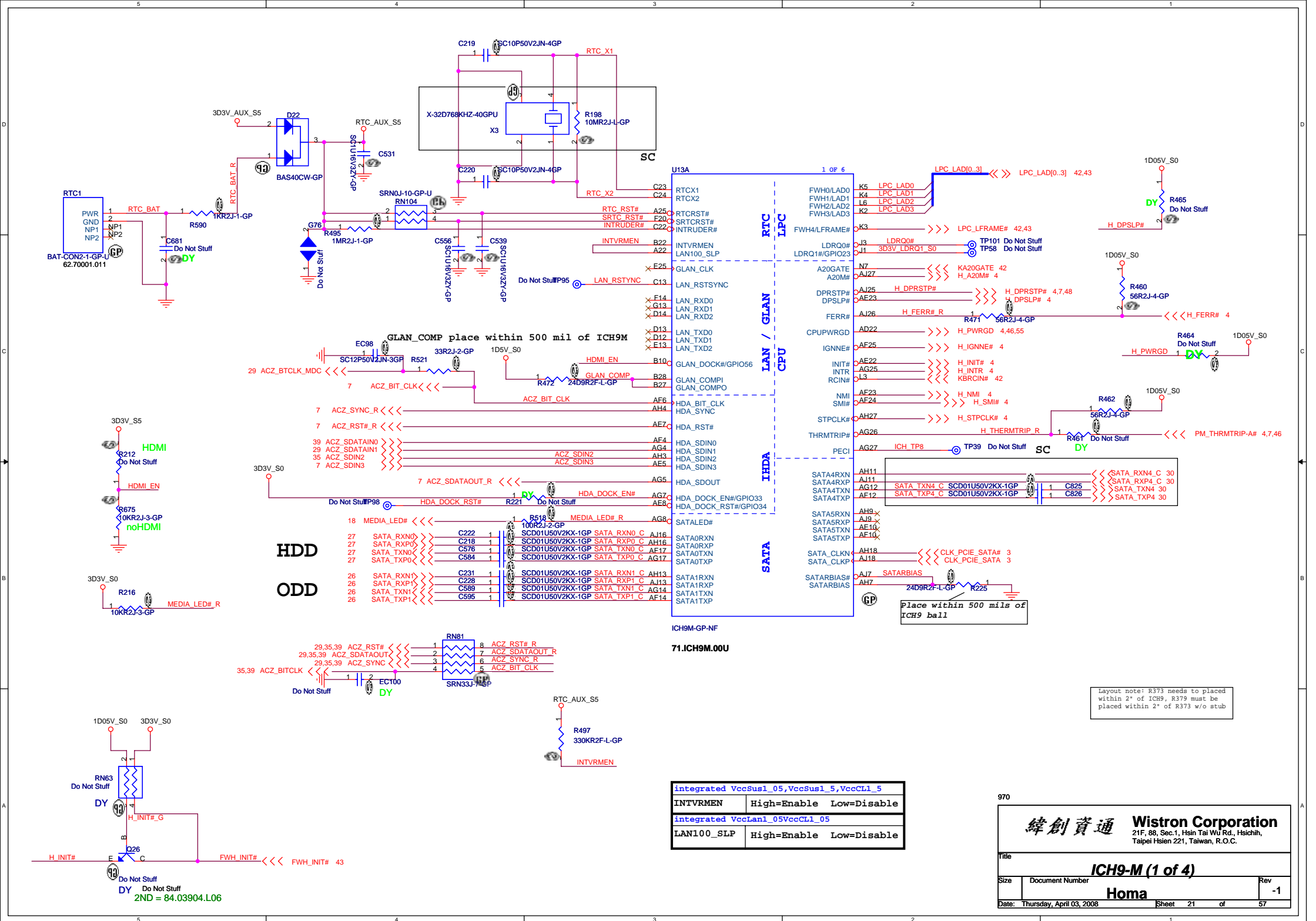
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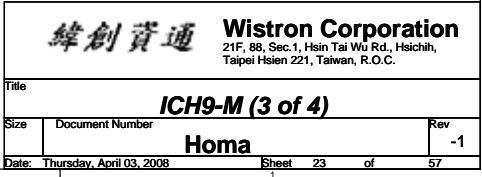
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Size	Document Number	Homa	Rev -1
Date: Thursday, April 03, 2008	Sheet 19	of 57	

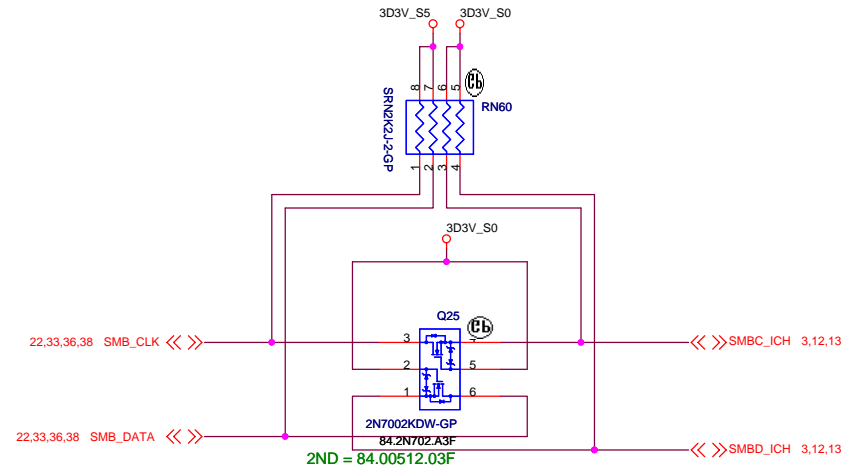
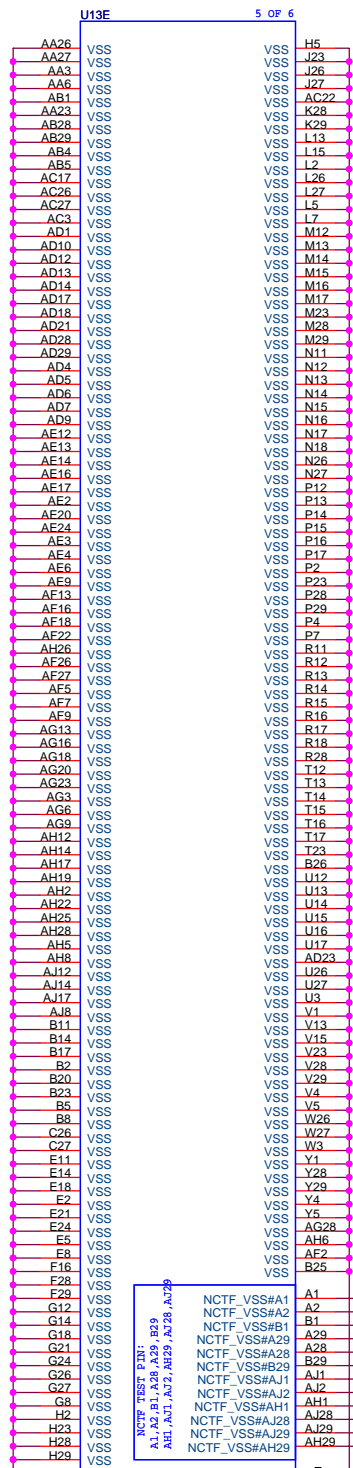


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Title			
HDMI CONNECTOR			
Size A3	Document Number Homa	Rev -1	
Date: Thursday, April 03, 2008	Sheet 20	of	57



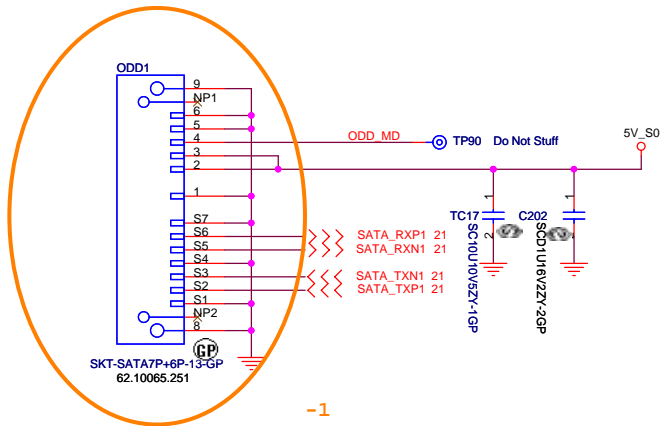




Q13 & Q14 connect SMLINK and
SMBUS in S) for SMBus 2.0
compliance

SMBUS

ODD Connector



970

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Title

CDROM

Size

Document Number

Homa

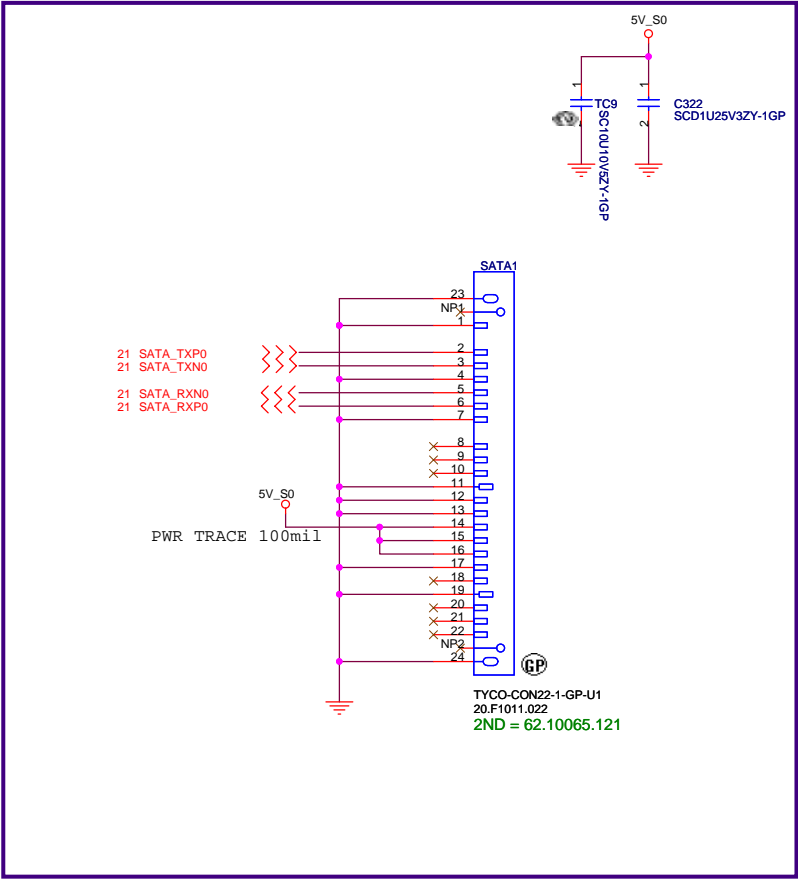
Rev

-1

Date: Thursday, April 03, 2008

Sheet 26 of 57

SATA Connector



The schematic shows the power supply for the Bluetooth module. A 3D3V_BT_S0 input is connected through a red wire to the OUT pin (pin 1) of the U22 voltage regulator. The IN pin (pin 5) of U22 is connected to the 3D3V_S0 input through a red wire and a capacitor C321. The GND pin (pin 2) of U22 is connected to ground. The EN pin (pin 4) of U22 is connected to the BLUETOOTH_EN signal through a red wire. The output of the regulator is labeled 1ST = 74.09711.A7F.

2ND = 20.F0984.004
20.D0197.104
ACES-CON4-1-GP-U2
BLUE1

3D3V_BT_S0

USBPN5

USBPP5

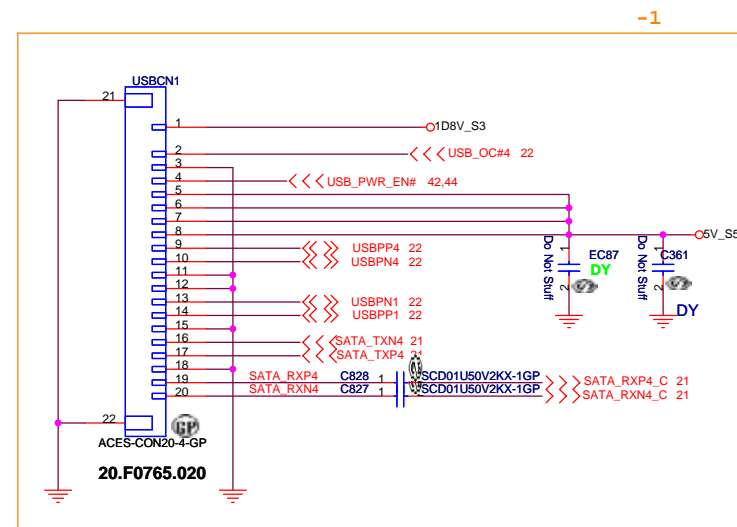
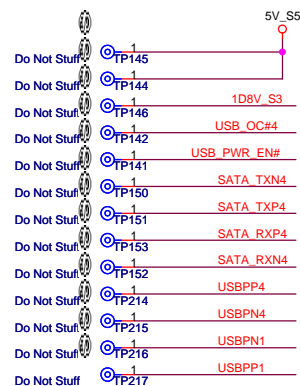
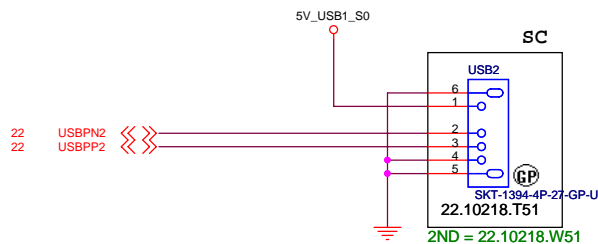
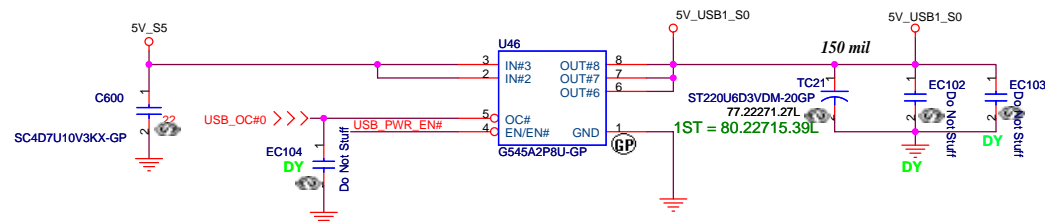
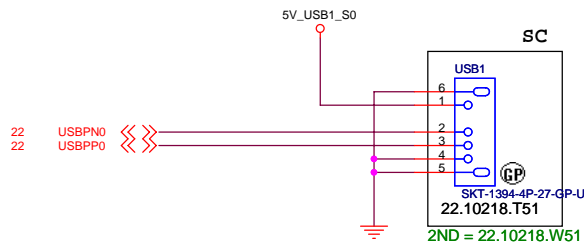
3D3V_BT_S0

Do Not Stuff

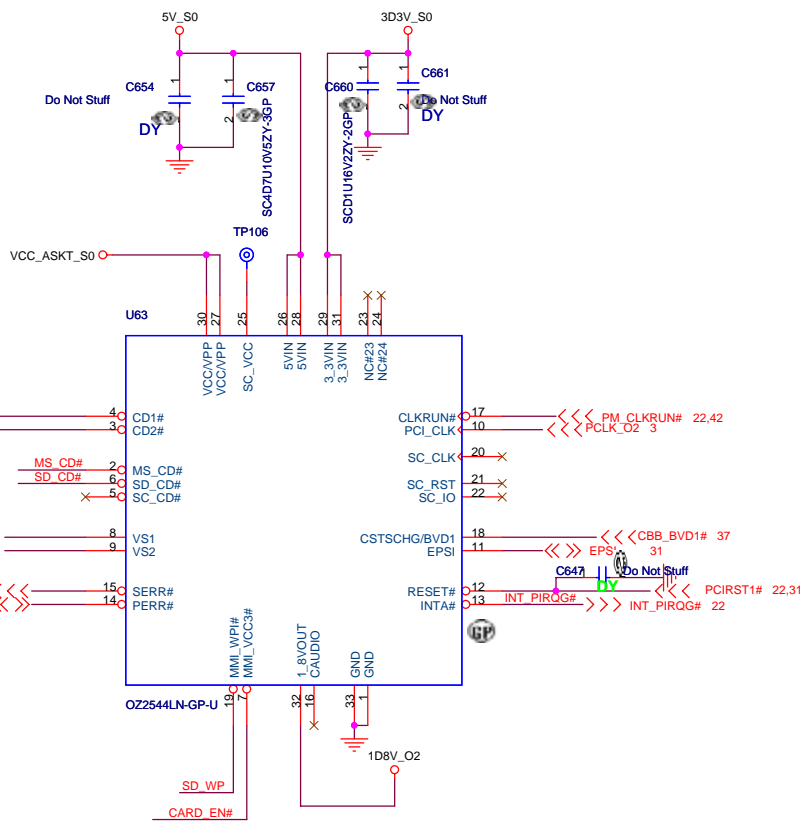
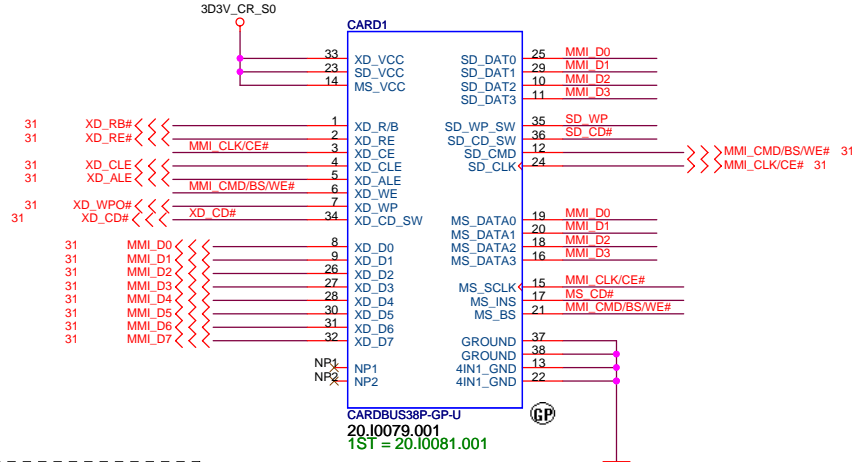
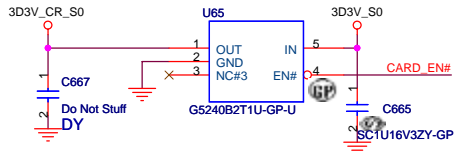
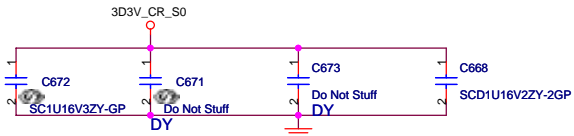
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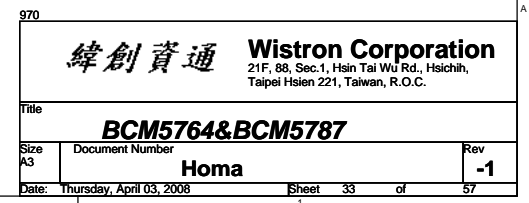
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[illegible]



**XD
MS / MS PRO
SD / SD IO / MMC**

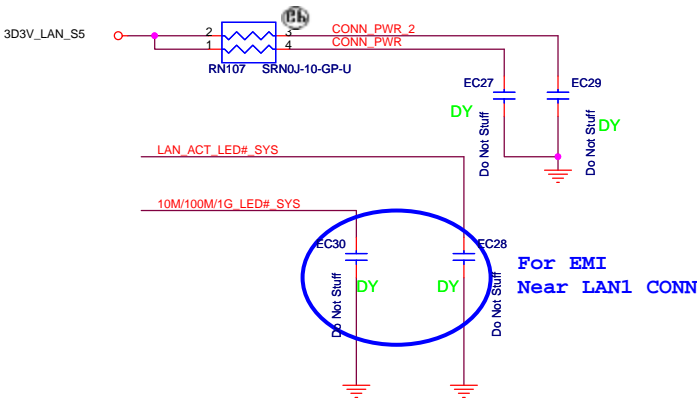
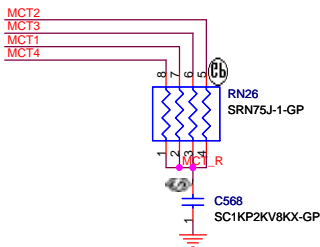
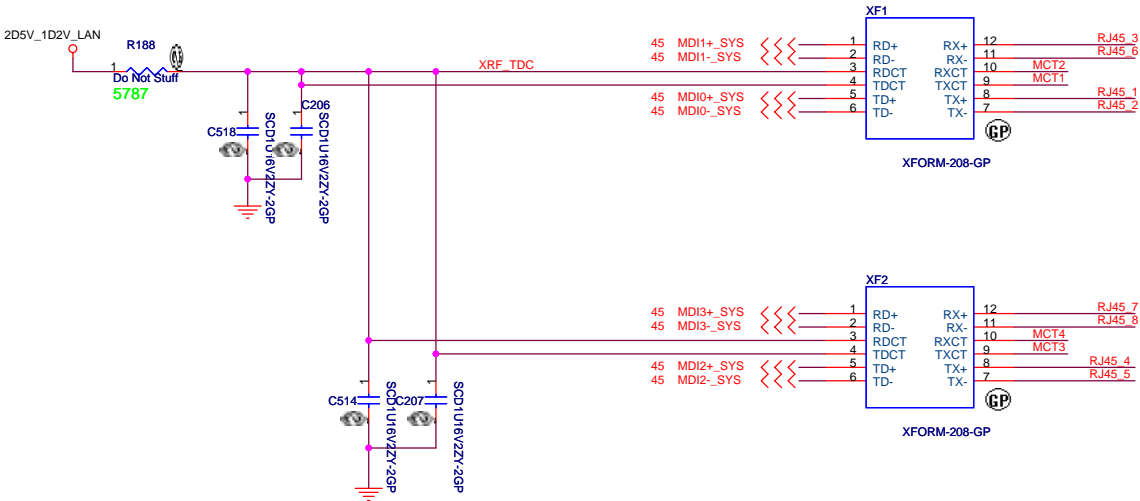




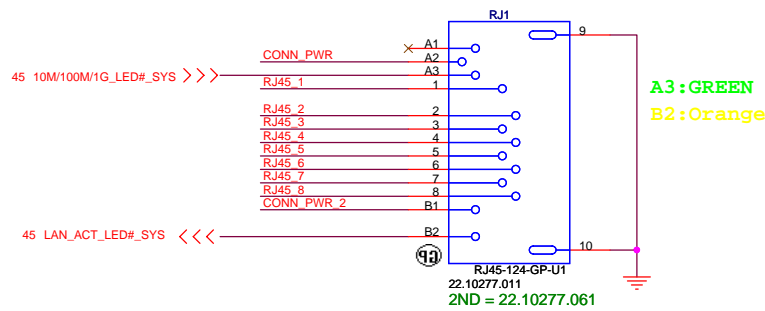
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

LAN Connector

GIGA Lan Transformer



LAN Connector

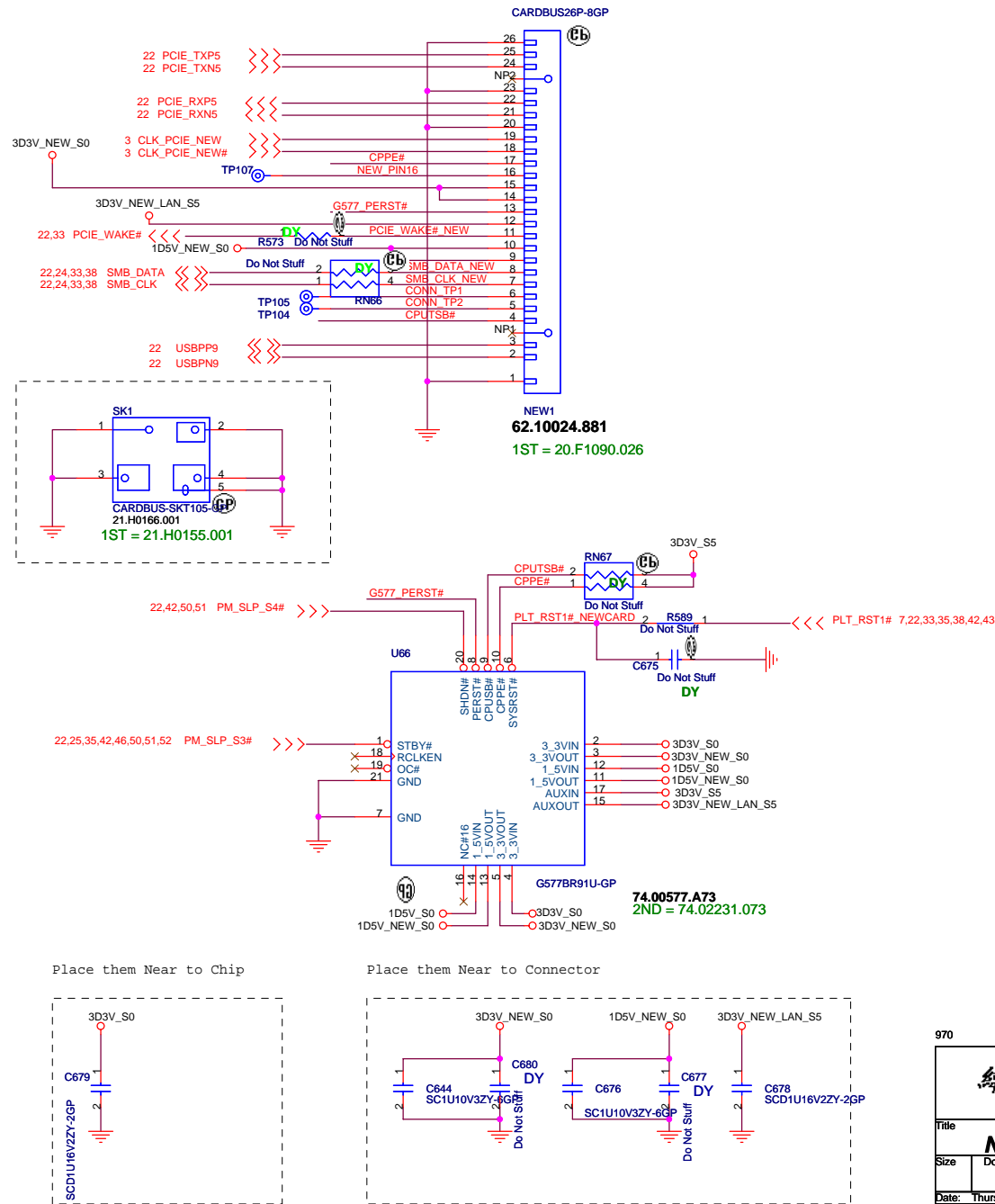


LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transferring data.

NEWCARD Connector

Reserve the symbol
for bottom side
connector



970

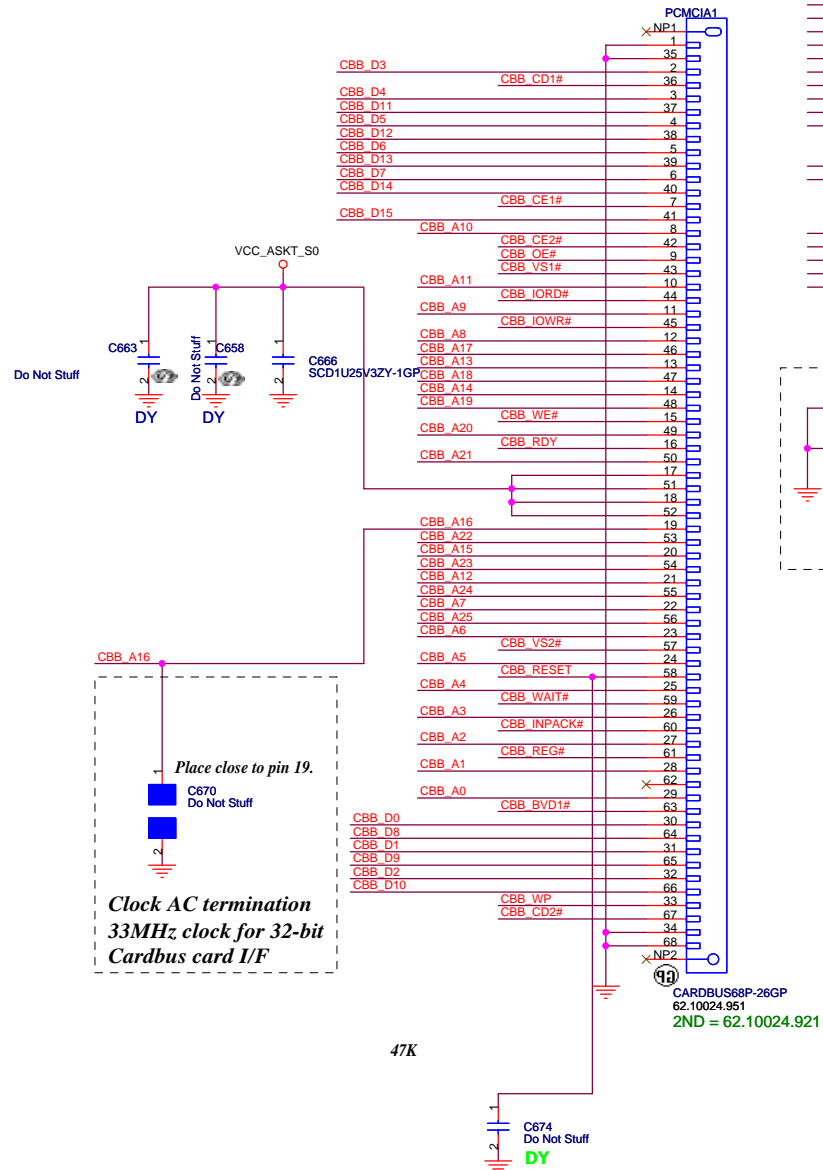
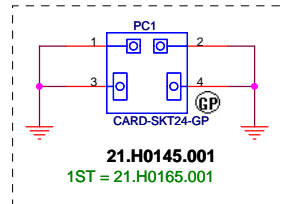
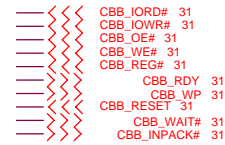
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

NEW CARD		
Size	Document Number	Rev
	Homa	-1
Date: Thursday, April 03, 2008	Sheet 36 of 57	

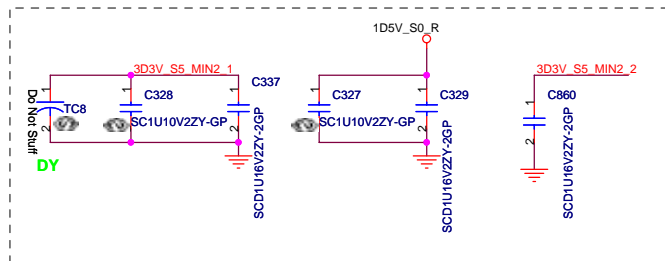
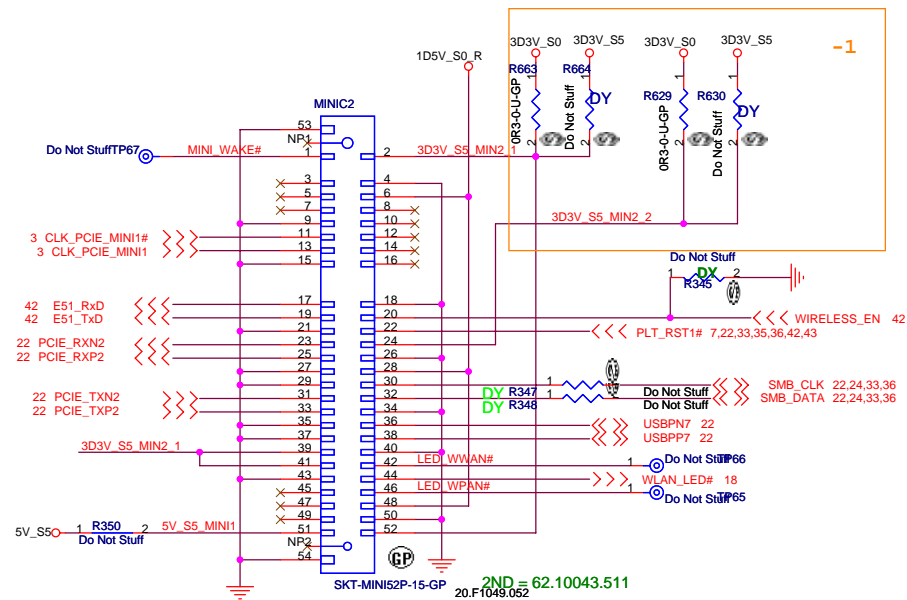
PCMCIA Socket

Cardbus I/F

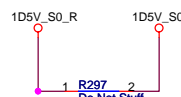
CBB_D[15..0] << >> CBB_D[15..0] 31
CBB_A[25..0] << >> CBB_A[25..0] 31



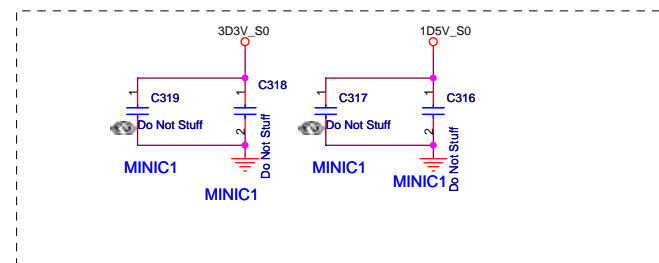
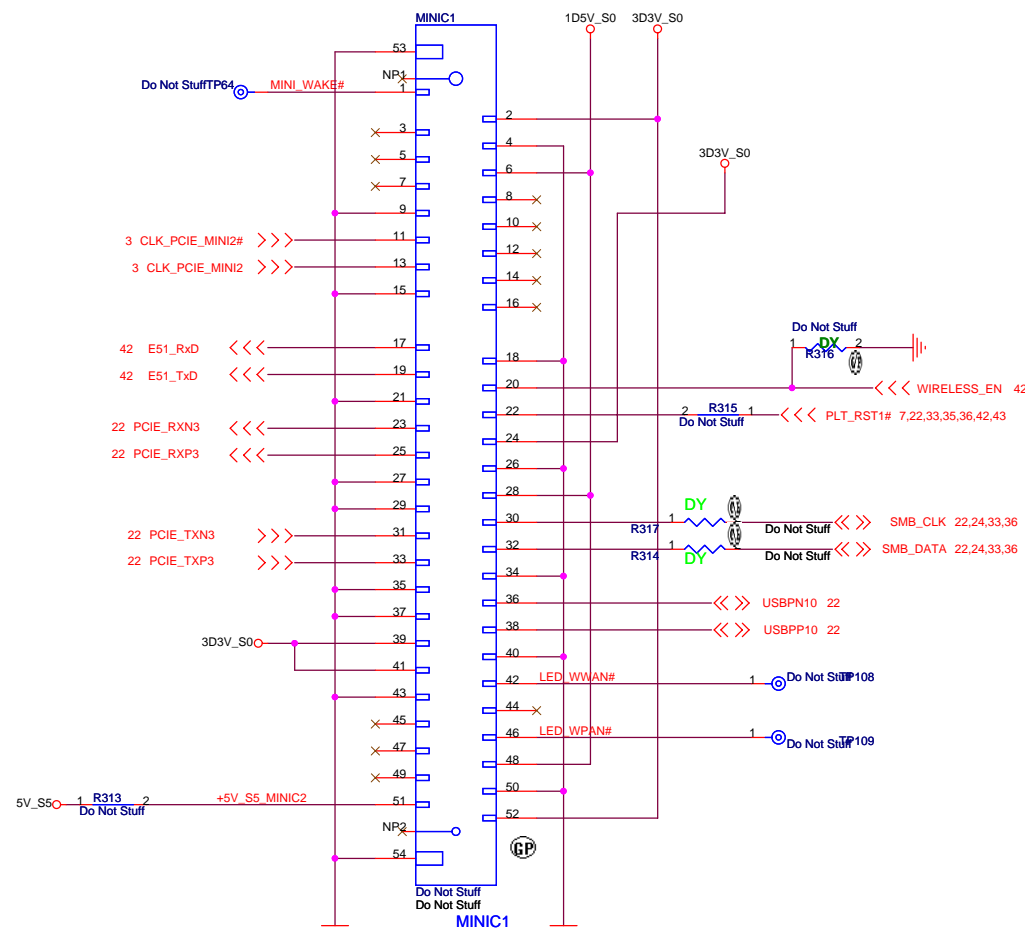
Mini Card Connector(WLAN)



Vo(cal.)=1.5024V OCP>3.2A



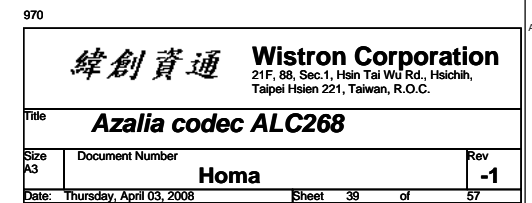
Mini Card Connector



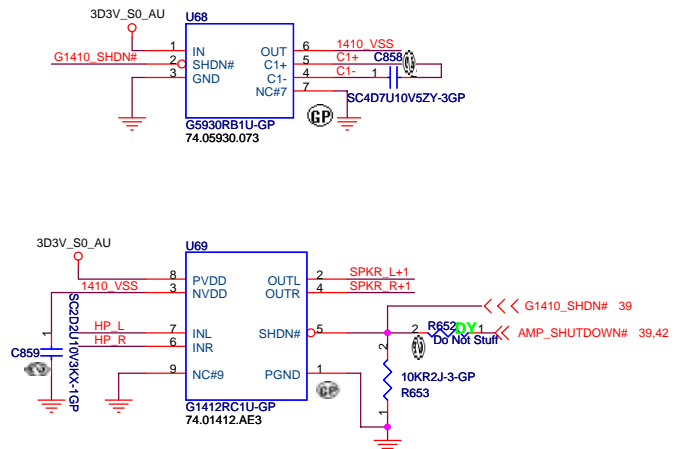
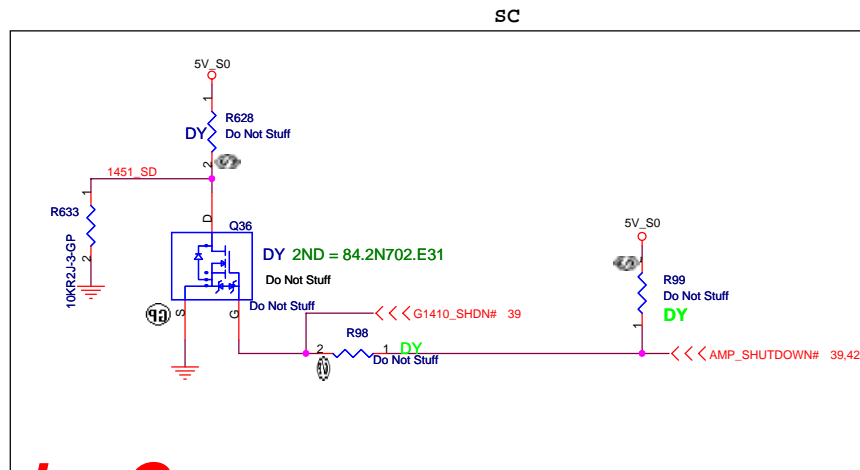
970

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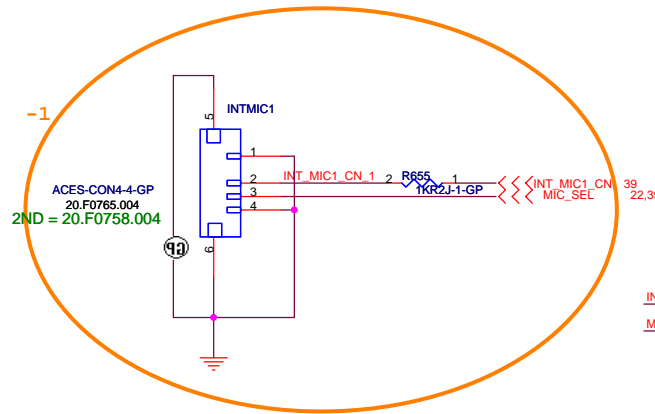
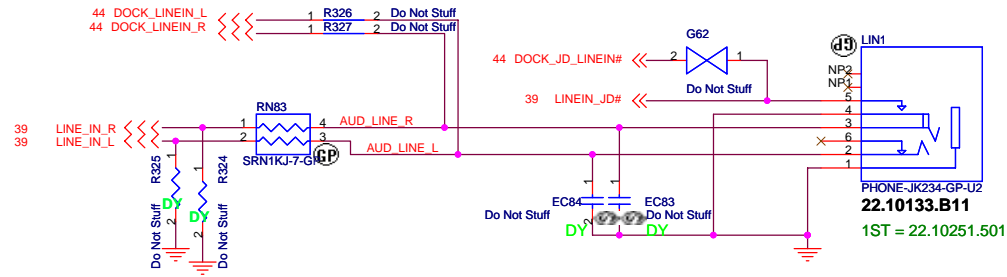
Title			MINI CARD	
Size	Document Number	Homa		Rev
A3				-1
Date:	Thursday, April 03, 2008	Sheet	38	of 57



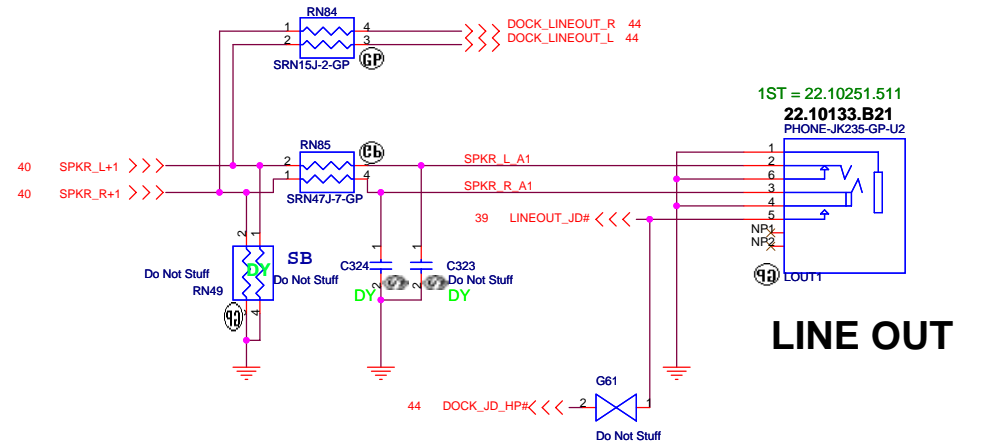
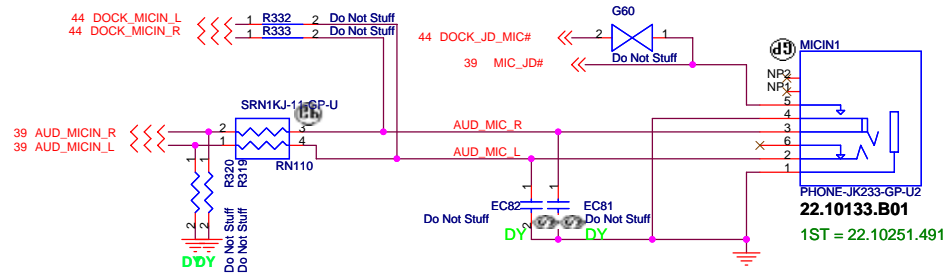
WWW.AliSaler.Com



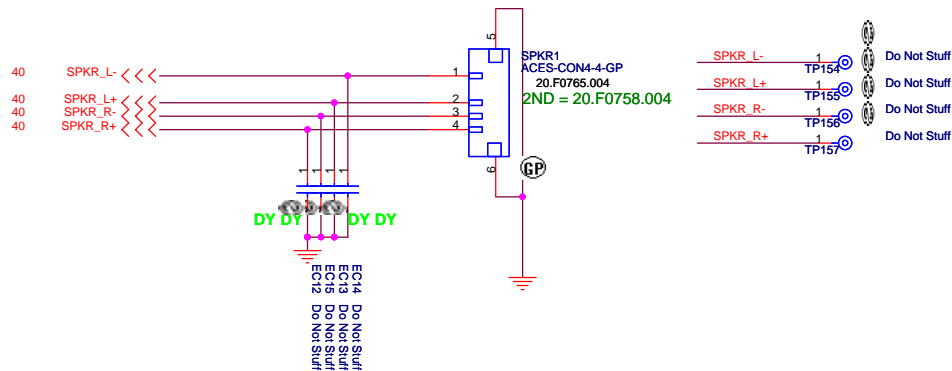
LINE IN



MIC IN



Internal Speaker

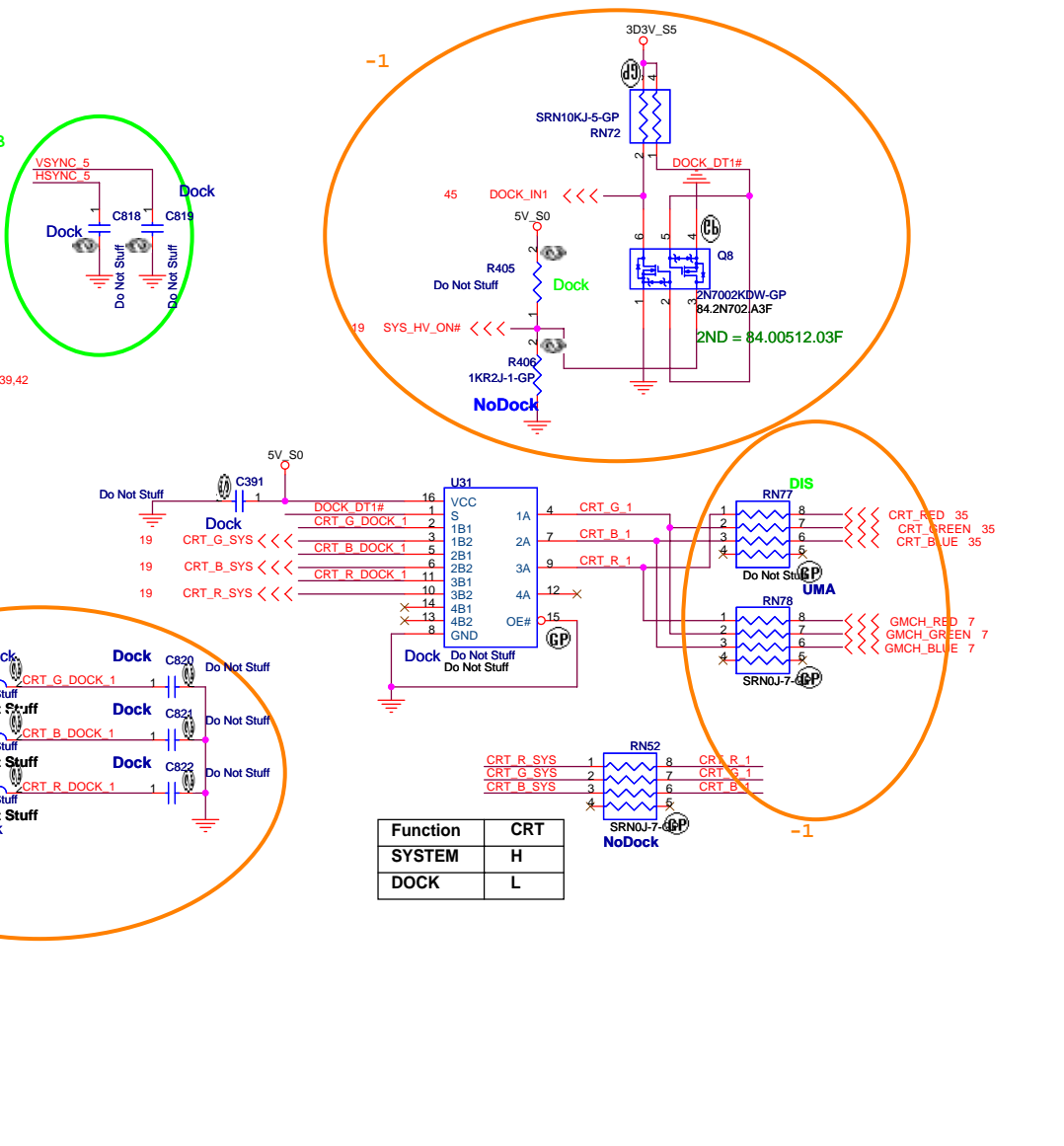
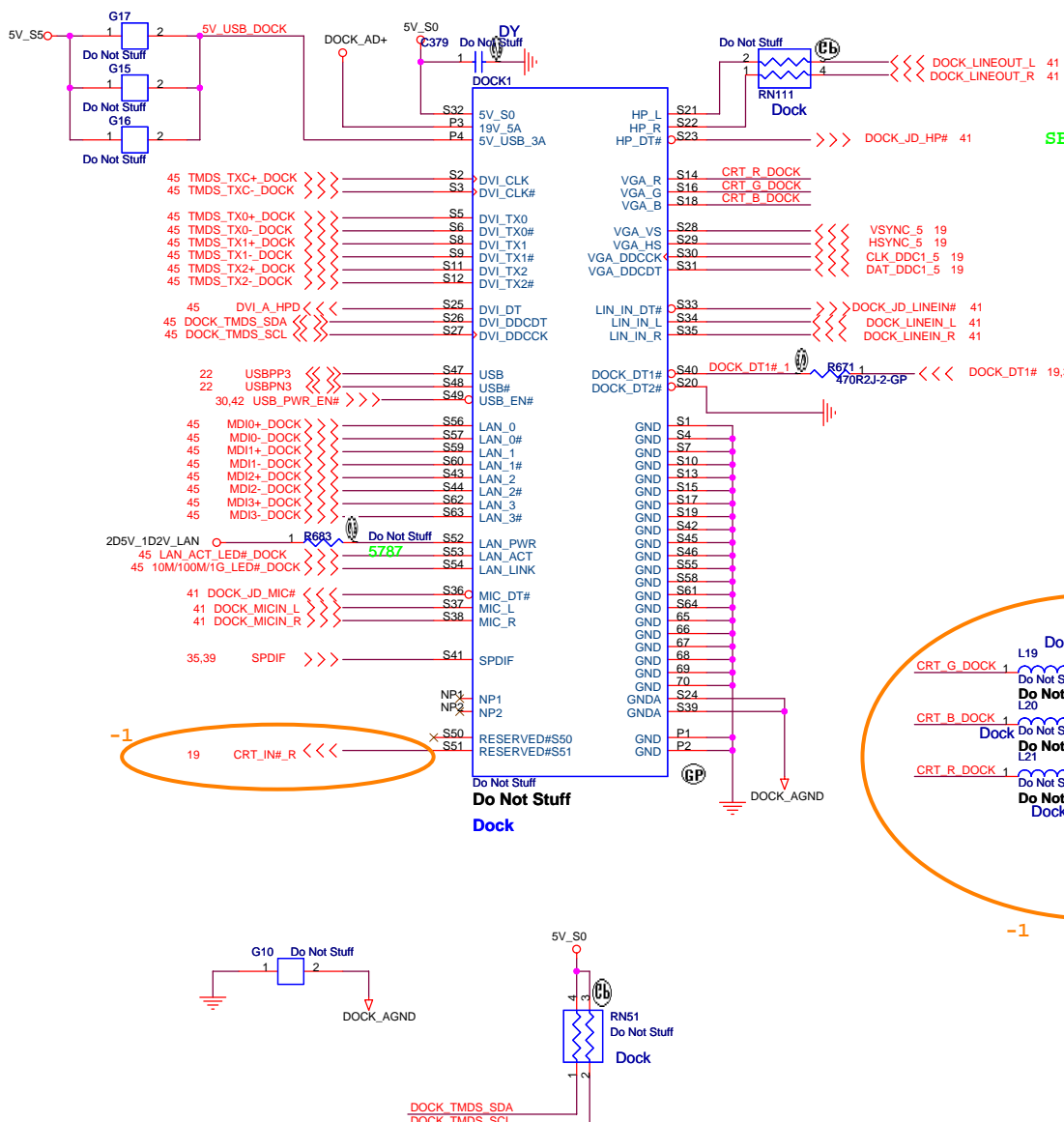


970

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Taipei Hsien 221, Taiwan, R.O.C.

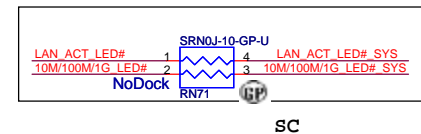
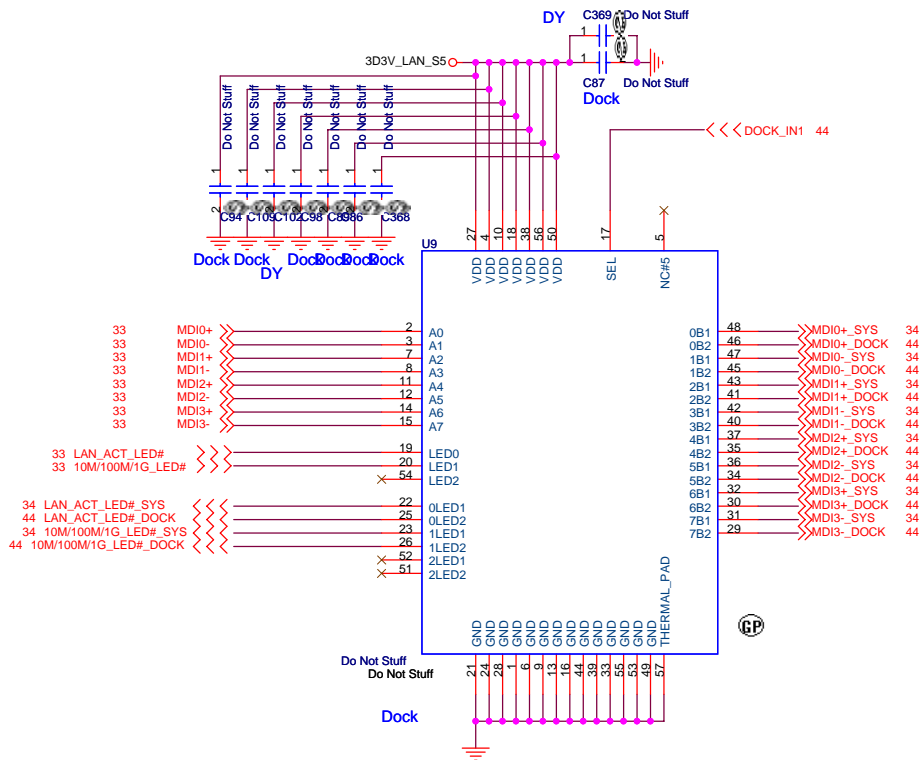
Title			AUDIO JACK
Size	Document Number	Homa	
Date: Thursday, April 03, 2008	Sheet	41	of 57

Rev -1

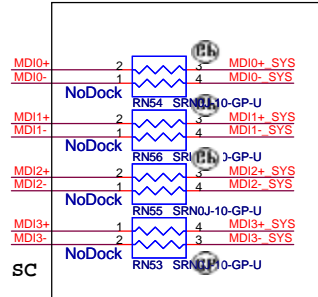


Function	CRT
SYSTEM	H
DOCK	L

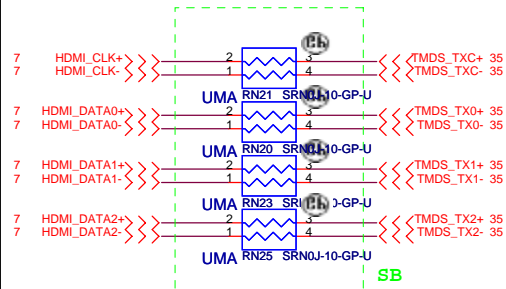
LAN switch



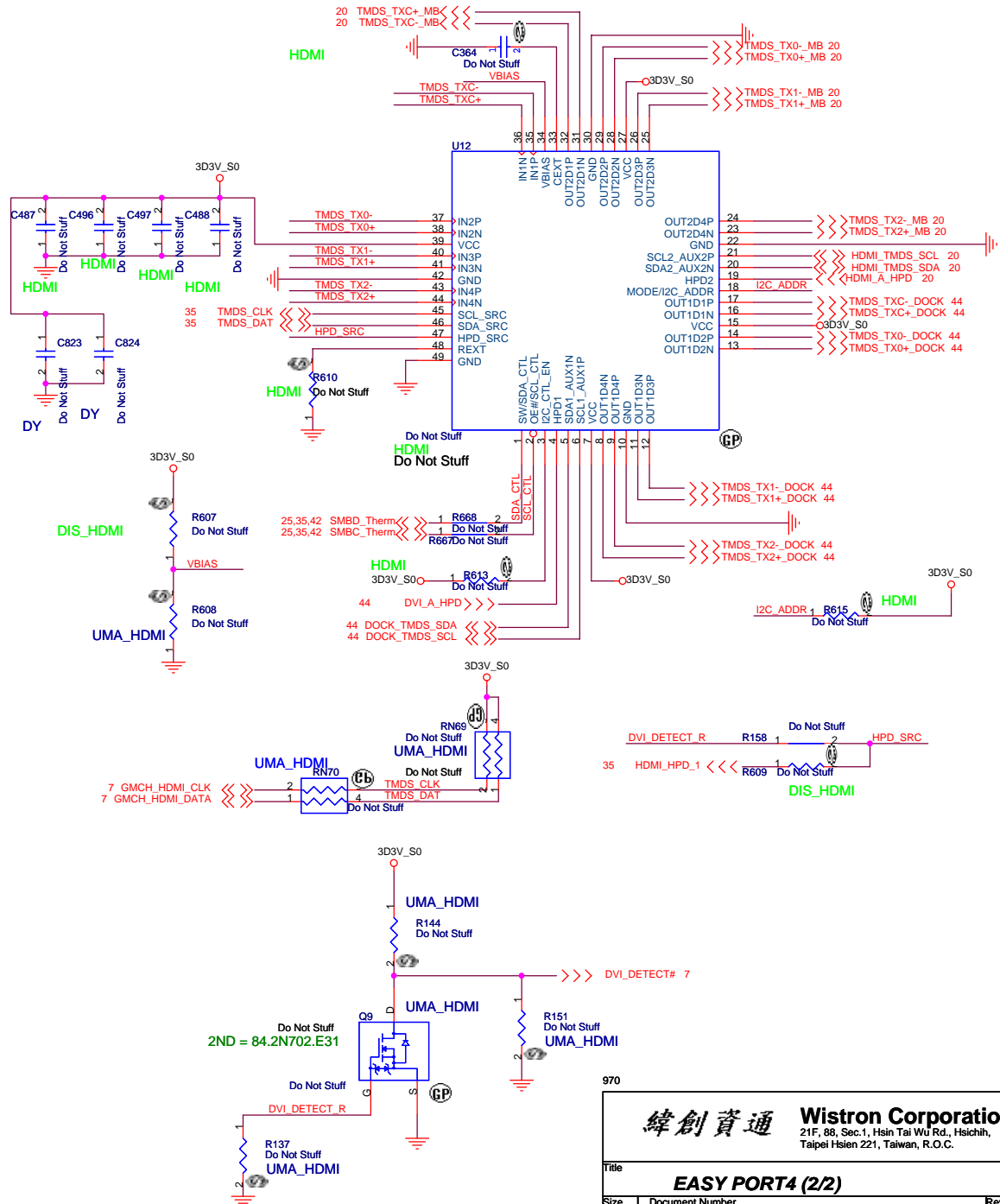
SC



SC

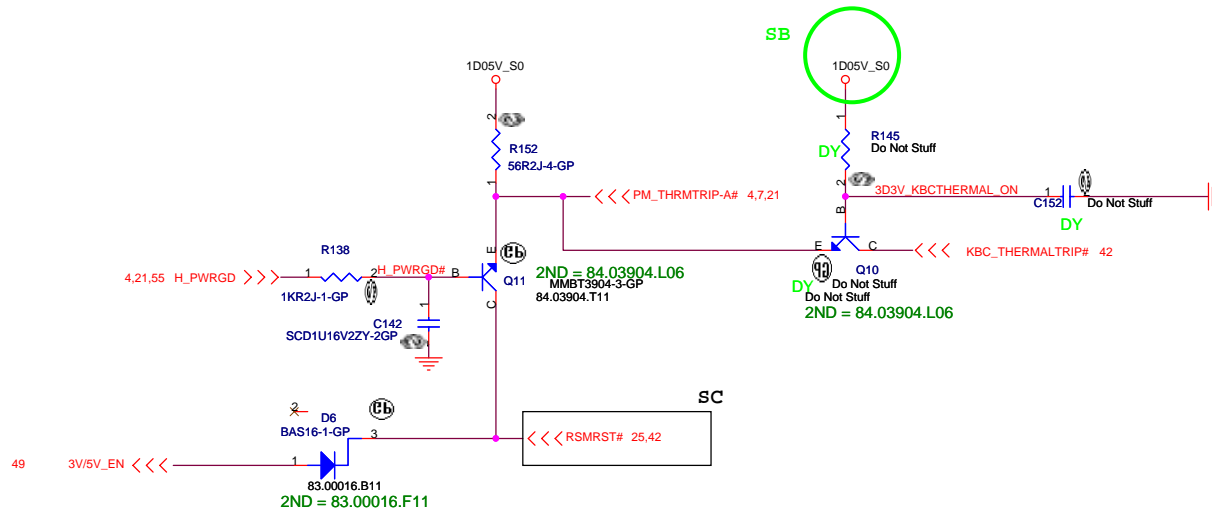
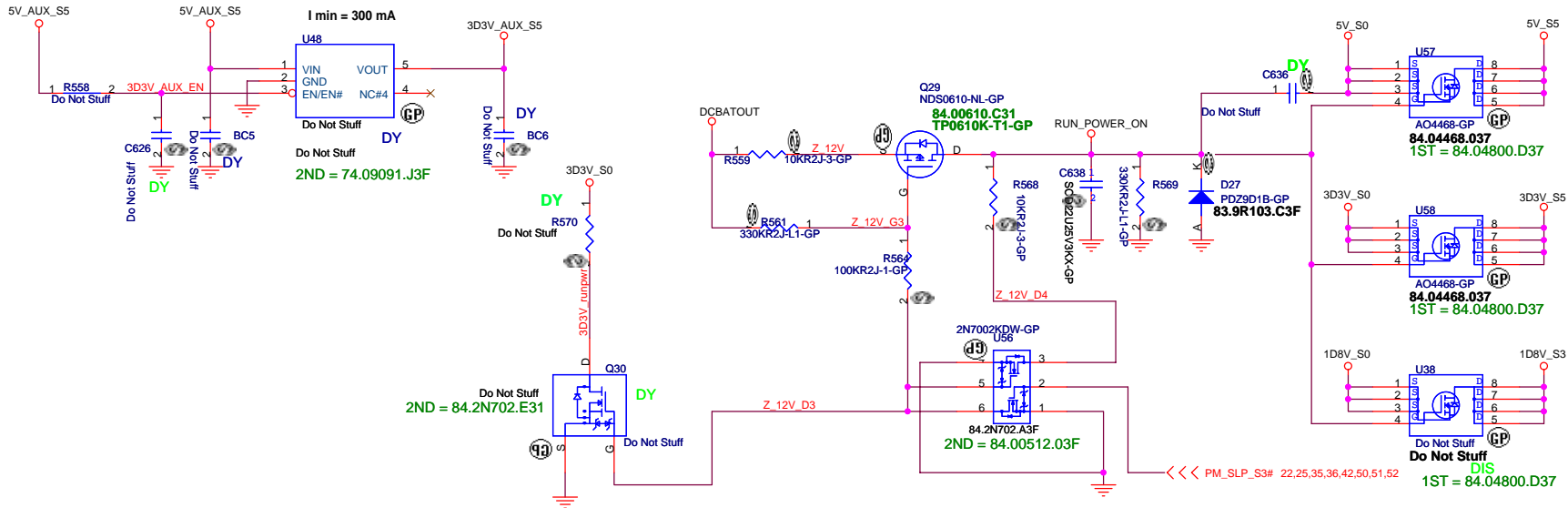


SB

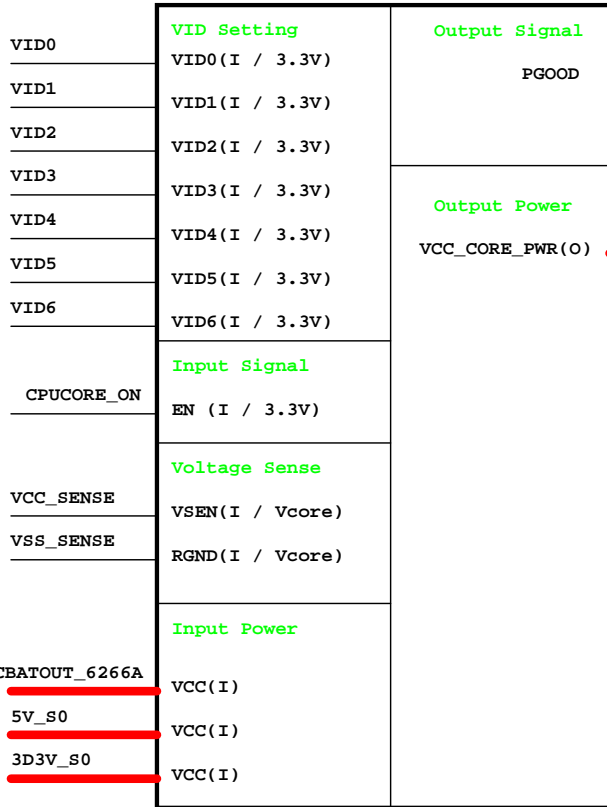


970

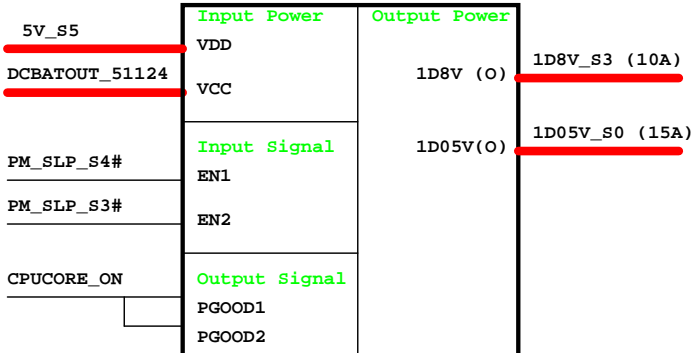
Run Power



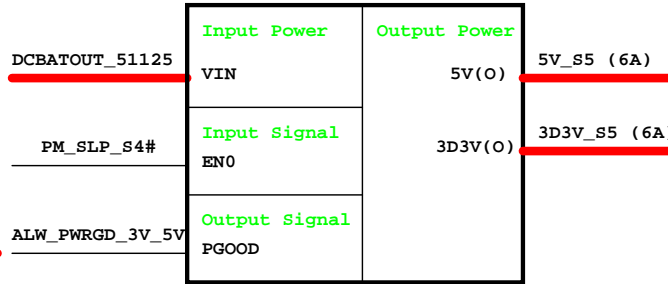
CPU_CORE
ISL6266A



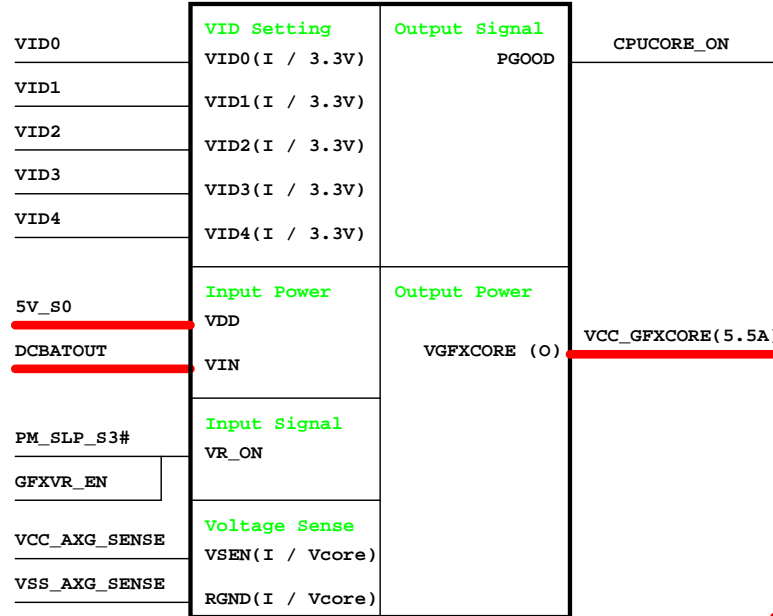
TPS51124
1D8V/1D05V



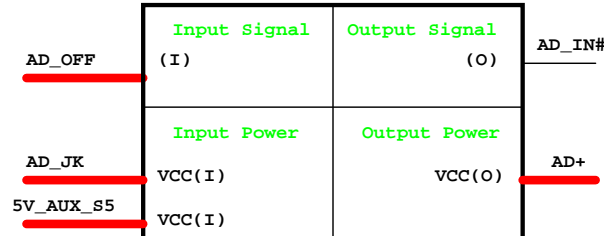
TPS51125
5V/3D3V



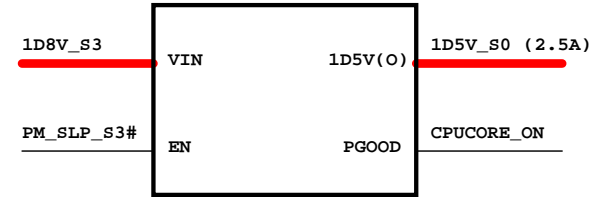
GFX_CORE
ISL6263A



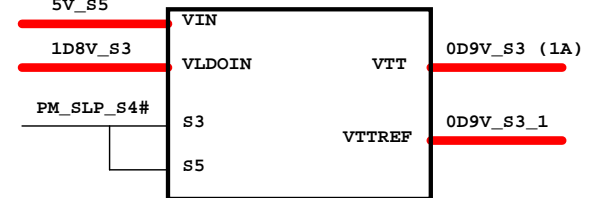
Adapter



RT9018A
1D5V_S0



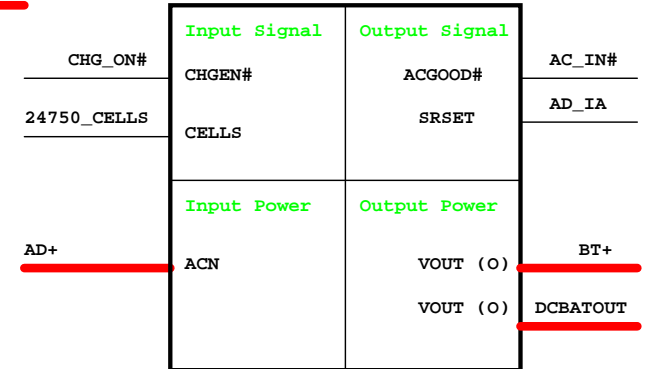
RT9026 0D9V_S0

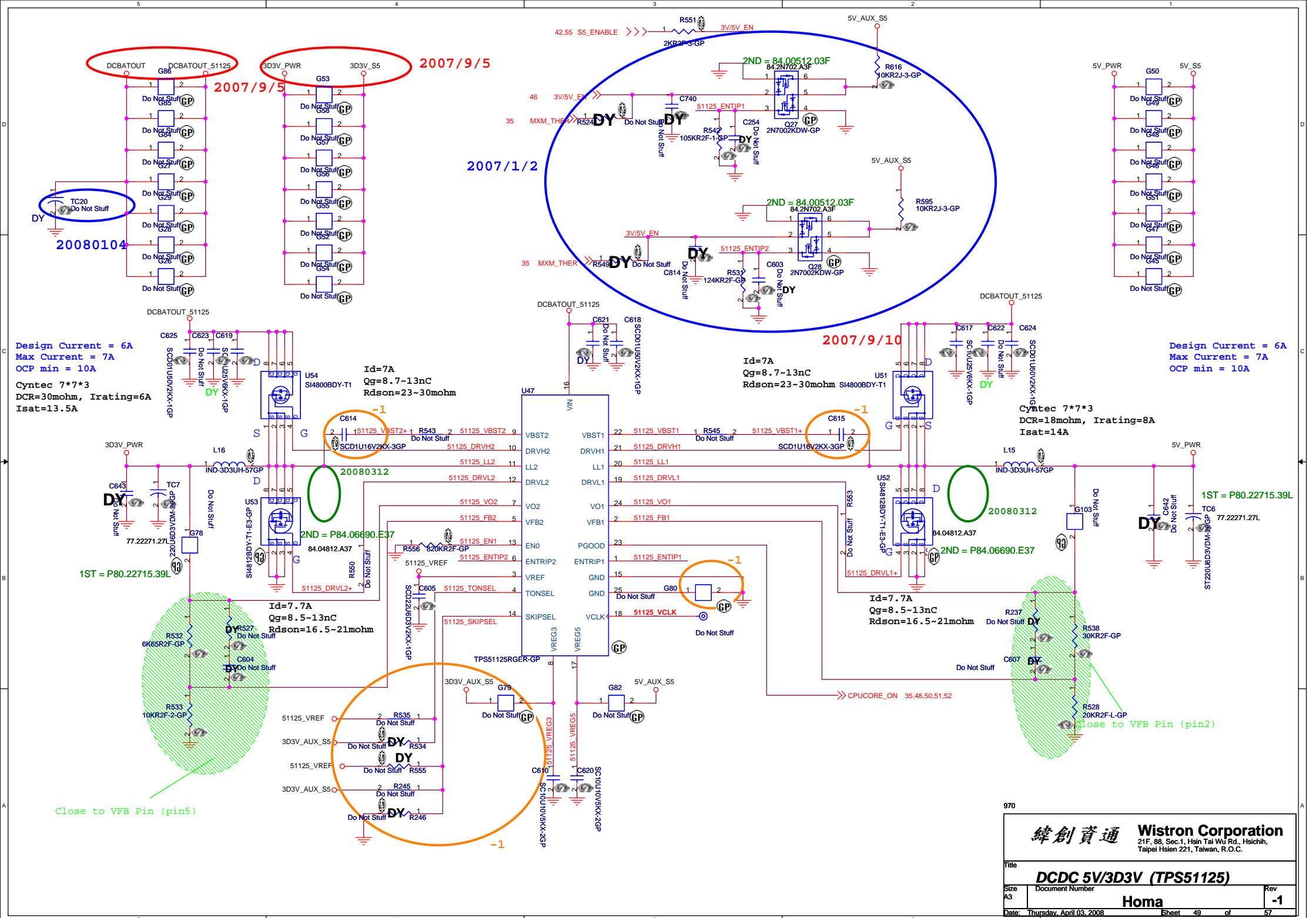


G9131 2D5V_S0

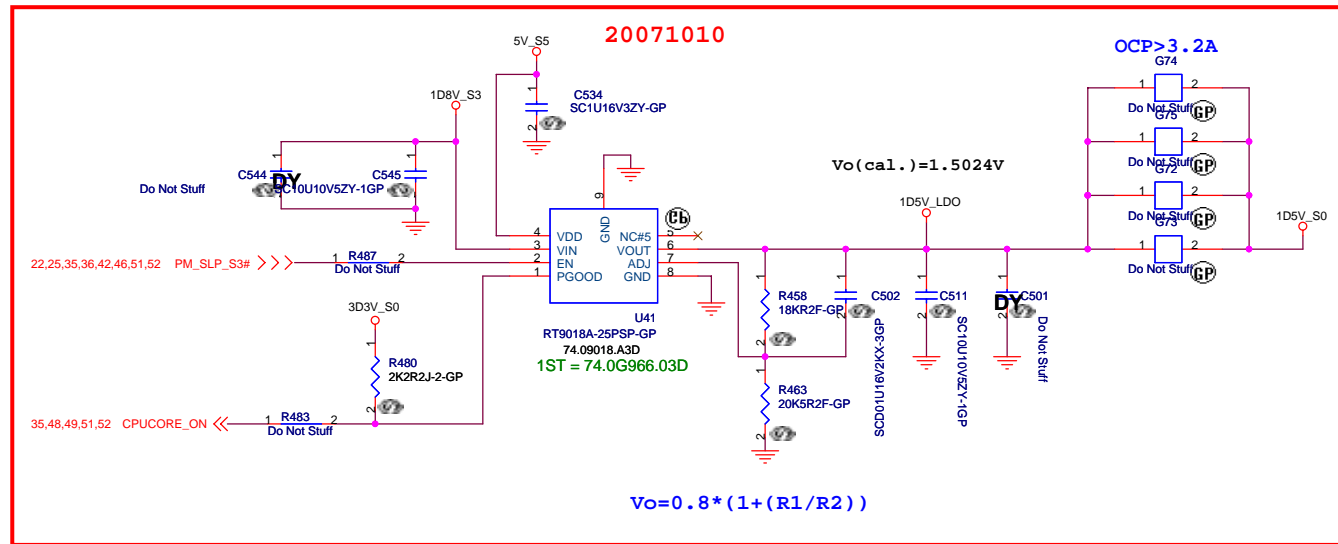


Charger BQ24750



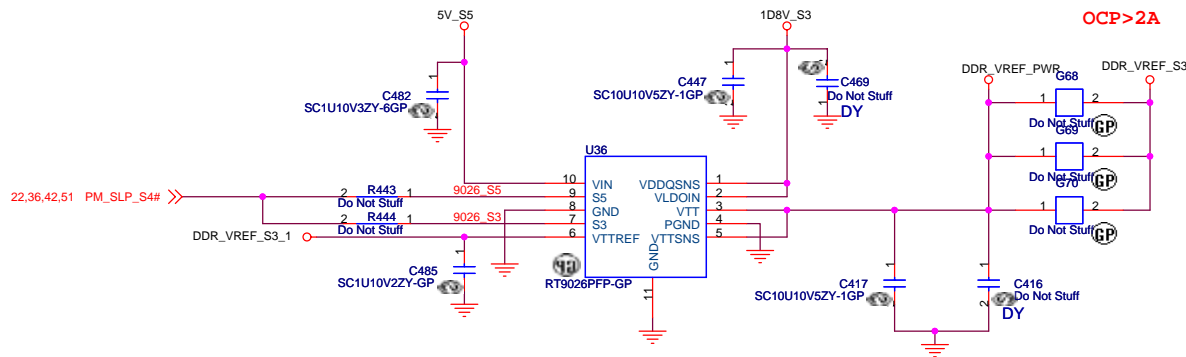


1D5V_S0
Iomax=2.5A

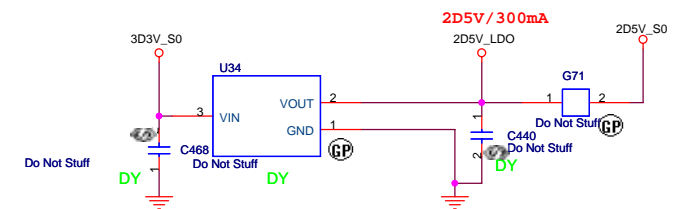


20071001

Iomax=1A
OCP>2A



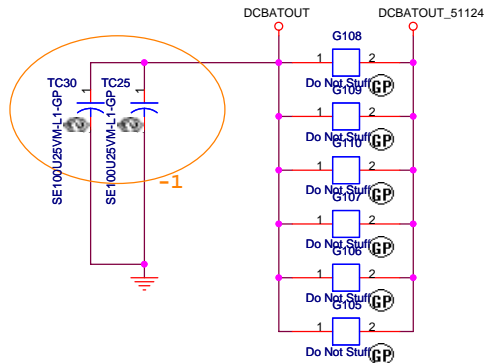
2D5V_S0
Iomax=0.3A



970

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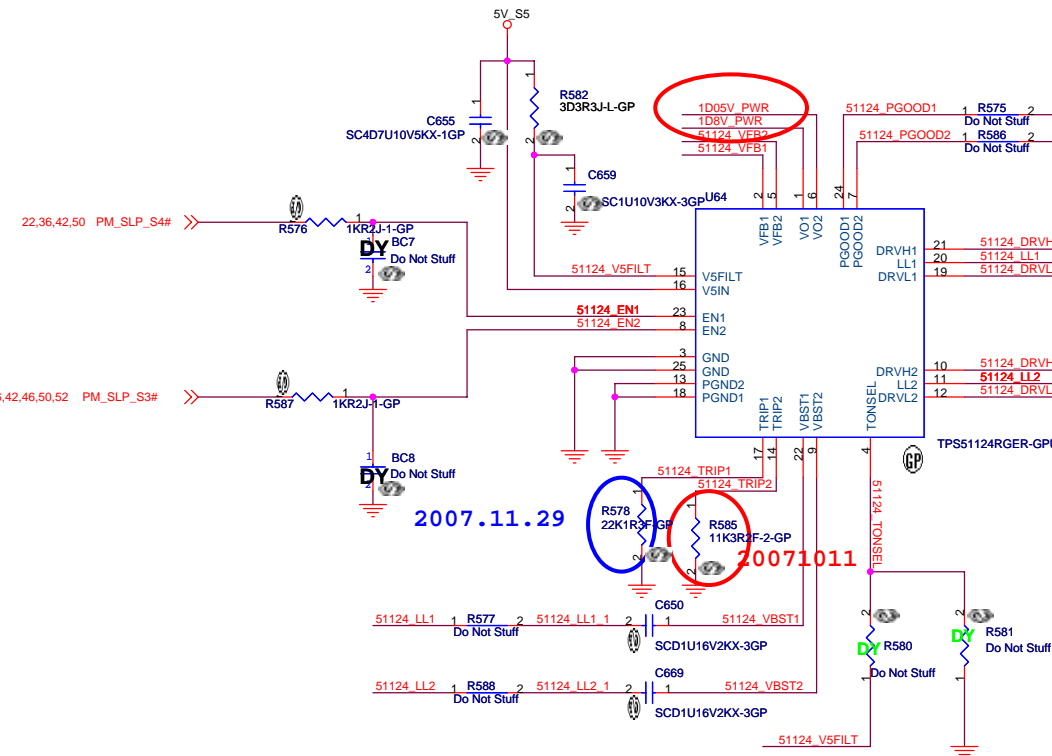
Title			
1D5V & 0D9V & 2D5V			
Size	Document Number	Rev	
A3		Homa	
Date:	Thursday, April 03, 2008	Sheet	50 of 57



$$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out}) / V_{in})$$

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L



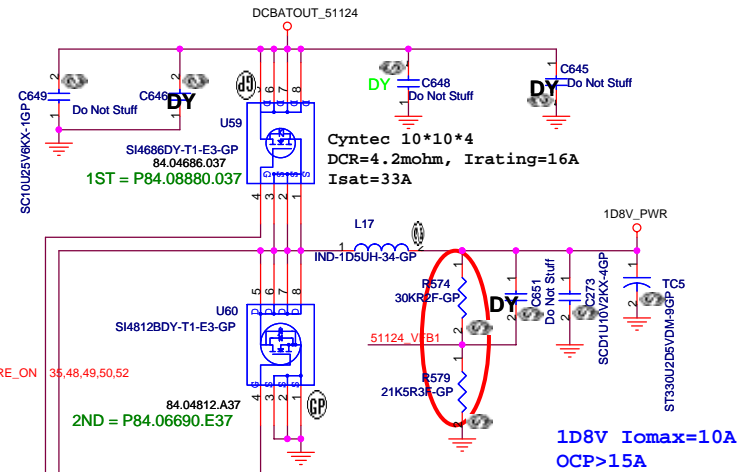
2007.11.29

20071011

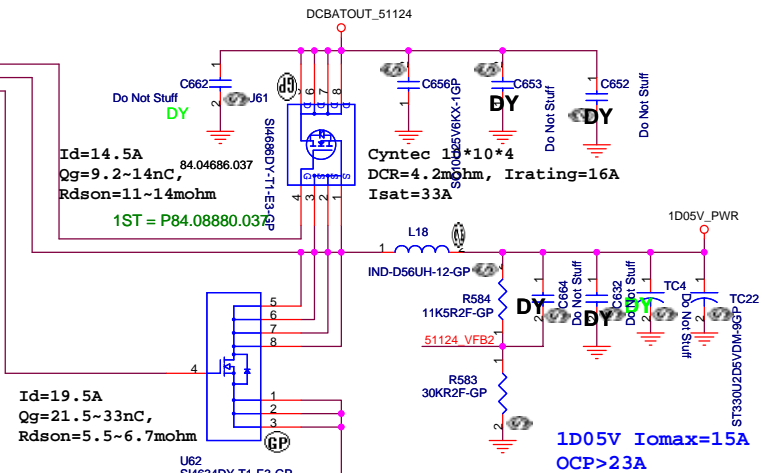
	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$$V_{out} = 0.758V * (R1 + R2) / R2 \text{ --> PWM mode}$$

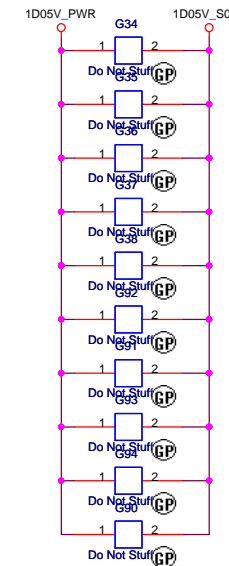
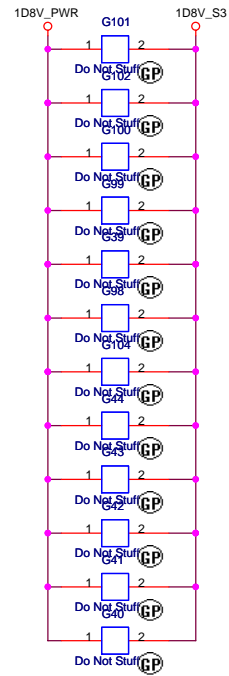
$$V_{out} = 0.764V * (R1 + R2) / R2 \text{ --> Skip Mode}$$



1D8V Iomax=10A
OCP>15A



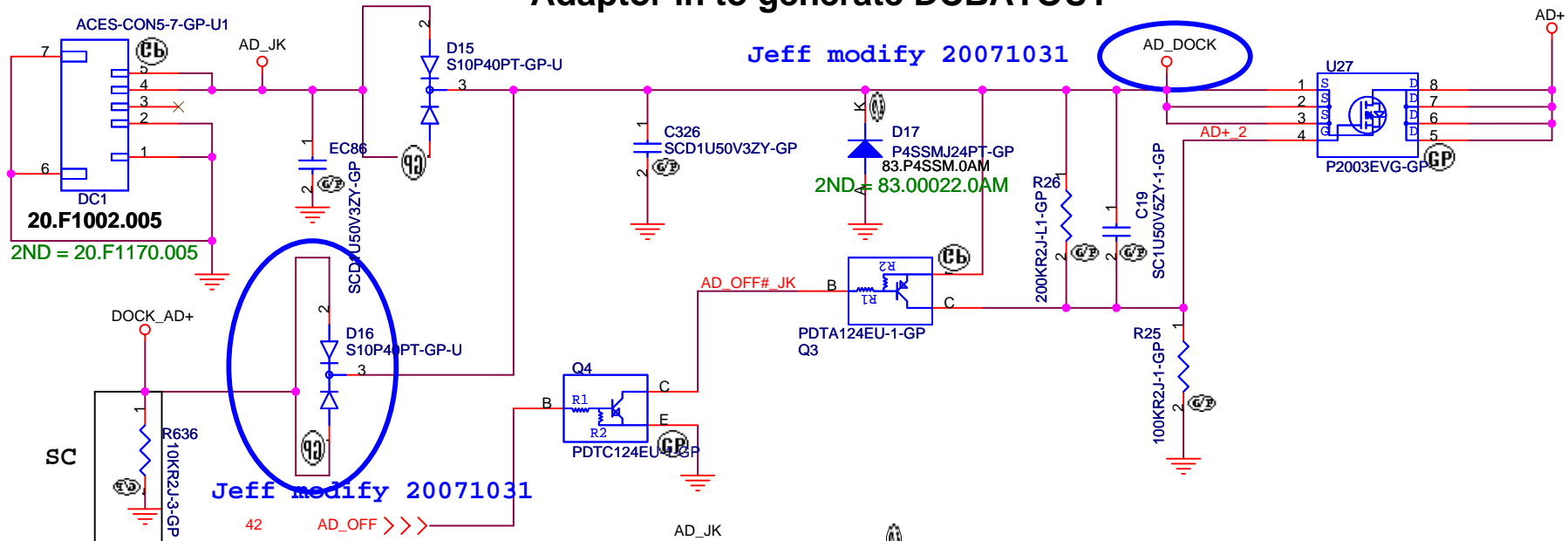
1D05V Iomax=15A
OCP>23A



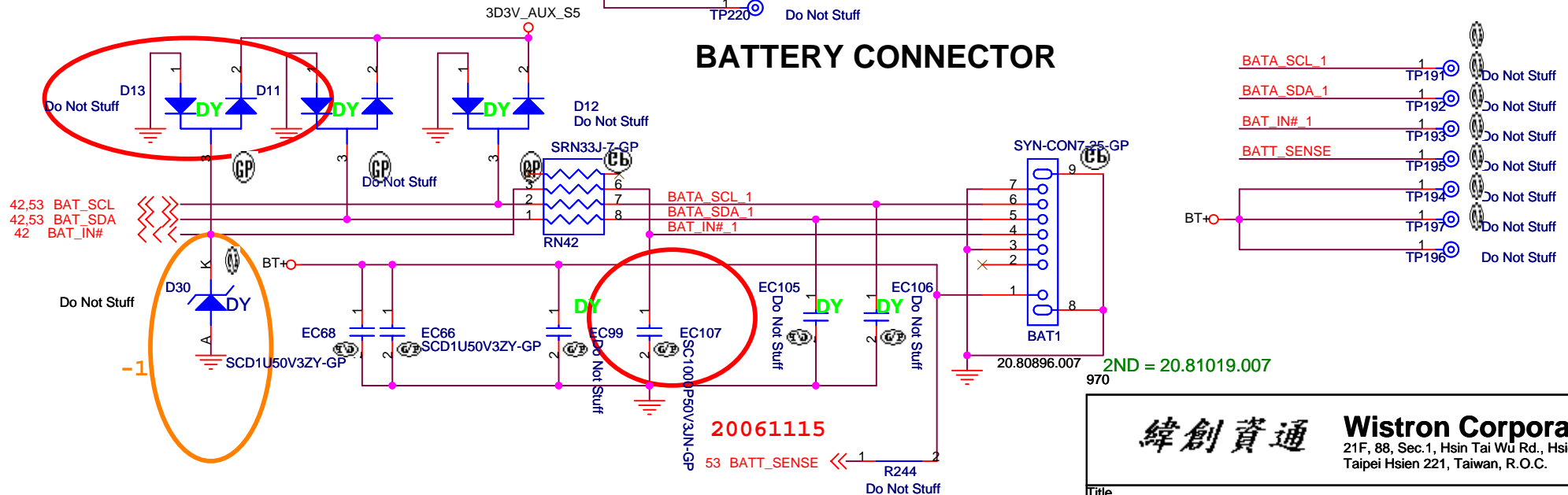
970

Adaptor in to generate DCBATOUT

Jeff modify 20071031



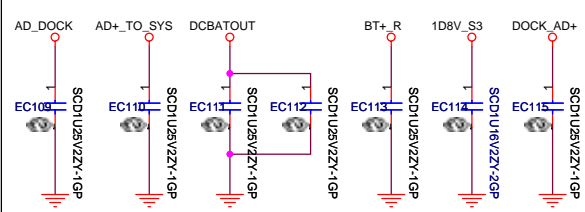
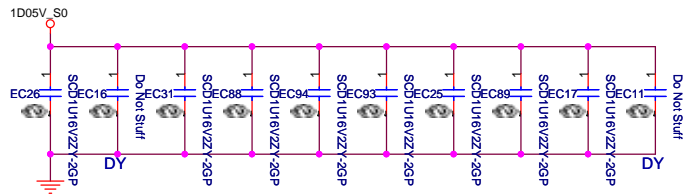
BATTERY CONNECTOR



緯創資通

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Title				
AD/BATT CONN				
Size	Document Number			Rev
	Homa			-1
Date:	Thursday, April 03, 2008		Sheet 54 of	57



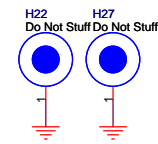
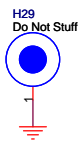
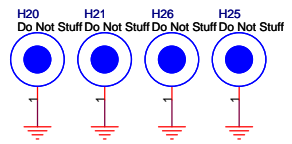
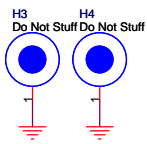
Check test point

- 3D3V_S0 <<< TP110 Do Not Stuff
- 3D3V_AUX_S5 <<< TP111 Do Not Stuff
- 3D3V_S5 <<< TP112 Do Not Stuff
- 5V_S5 <<< TP113 Do Not Stuff
- 22,42 PM_PWRBTN# <<< TP114 Do Not Stuff
- 4,21,46 H_PWRGD <<< TP115 Do Not Stuff
- 42,49 S5_ENABLE <<< TP116 Do Not Stuff
- 4,6 H_CPURST# <<< TP117 Do Not Stuff

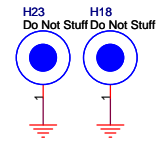
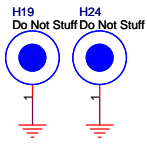
Test Point 放在 Dimm Door 打開可量測處

Stand off Location

34.42Y01.031



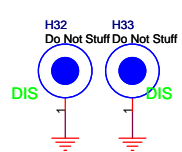
34.4G502.021



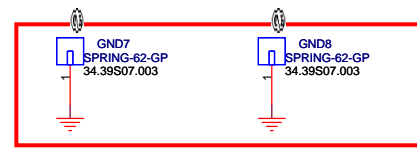
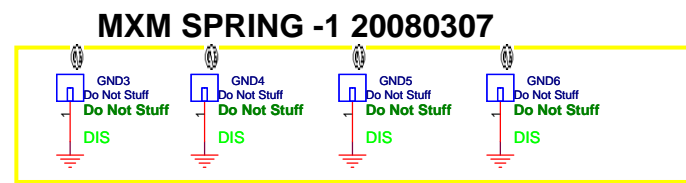
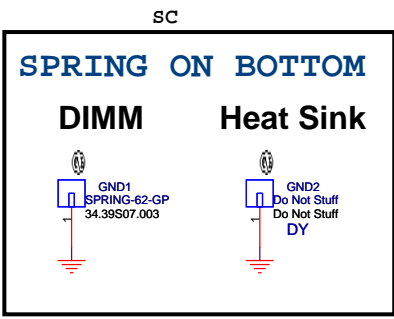
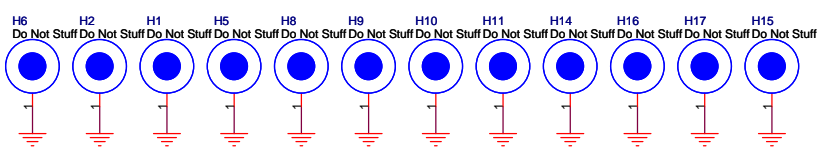
34.4Z402.011



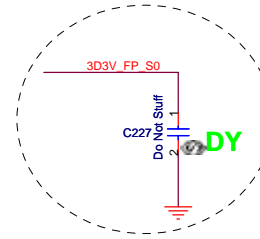
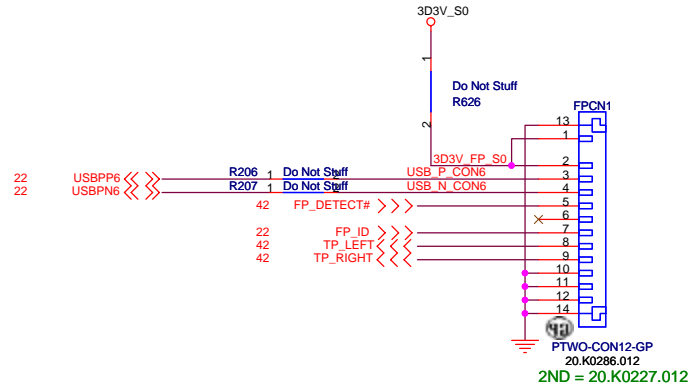
34.4Z401.011



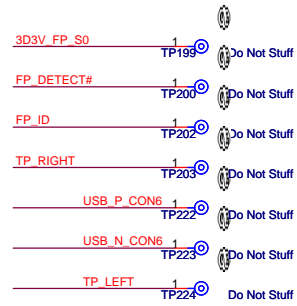
**DELETE MXM
STAND-OFF
H7;H28;H30;H31**



Finger printer



For EMI



970


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Title			FP	
Size	Document Number	Homa		Rev
A3				-1
Date:	Thursday, April 03, 2008	Sheet	56	of 57

SA --> SB

- 1.page25,Change Q24 and Q5 Pin_C and Pin_E net, Swap H_THERMDA and H_THERMDC(only close to C95)
- 2.page46,Change R145_Pin1 pull hige power to 1D05V_S0
- 3.page42,Add the Net let link U17_Pin101 and RN45_Pin3
- 4.page16,SWITCHCN1 pin12 connect to 3D3V_AUX_S5 and pin 11 connect to LID_CLOSE#
- 5.page20,HDMI1 change to 62.10078.171
- 6.page44,DOCK1 pin51 connect to CRT_DEC#
- 7.page53,R214 change to connect BQ24745_VREF as charger modify
- 8.page26,change ODD1 to 22.10300.141
- 9.page45,change U12 to PS8122QFN48G-GP and add some components
- 10.page44,Del U5
- 11.page20,Del U11,U42,Q9...
- 12.del G1-G8
- 13.page45,R614 changed to "DOCK_DT1#" and U12 output port1 and port2 swap,RN68 pin1&2 change to KBC SMBUS, RN69 pin3&4 change to connect"3D3V_S0",R615 change to 4K7R2F-GP
- 14.page49,change Q27&Q28 to 2N7002SPT ,add R595 R616
- 15.page48,change R12 to 10K2R3F-GP ,R13 to 16K5R2F-1-GP
- 16.page51,R578 change to 22K1R3-GP
- 17.page52,R257 change to 2K87R2F-1-GP ,C259 change to SCD033U50V
- 18.page40,change U8 to G1454R41U-GP
- 19.page42,Del R29 R27 C20 EC5
- 20.page41,LID1 change to INTMIC1 and connect to "MIC_L_CN"&"MIC_R_CN"
- 21.page39,add R619 C815 R621 R620 C816 C817
- 22.page38,Del C355 C320
- 23.page56,Del F4 addR626
- 24.page3,R204 change to connect"3D3V_CLKPLL_S0"
- 25.page52,add R622~R625
- 26.page44,add C818~C822 and L19 L20 L21
- 27.page35,Del TP77~TP82 TP84 TP86 TP87 TP24 TP25 TP26 TP28,add R618 pull up to 3D3V_S0
- 28.page25,add R617 Q35 del R115
- 29.page30,change C600 to 4.7U10V
- 30.page45, swap U12 output port1&pot2
- 31.page48~52, change power GAPs to close GAPs
- 32.page49,L15 change to 1ND-3D3UH by power modify
- 33.page16,add R627 EC108
- 34.page45,add C823 C824 and R144 R151 Q9 R137

970



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Title

Change list

Size
A3

Document Number
Homa

Rev
-1

Date: Thursday, April 03, 2008

Sheet 57 of 57